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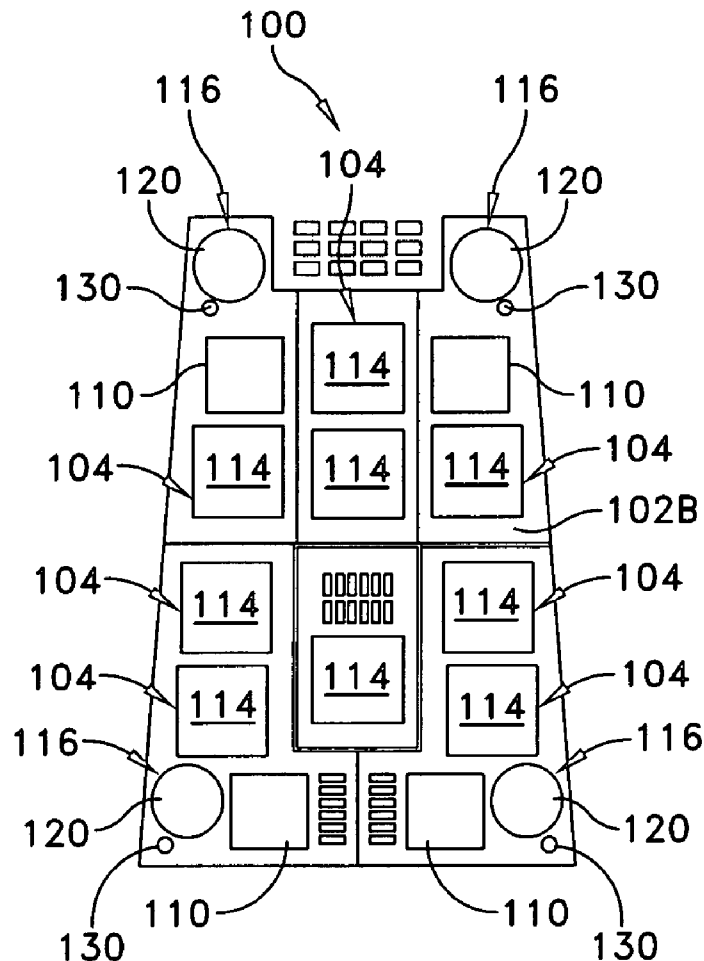
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(19) **United States**(12) **Patent Application Publication**
Mayder et al.(10) **Pub. No.: US 2007/0247140 A1**(43) **Pub. Date: Oct. 25, 2007**(54) **APPARATUS, SYSTEMS AND METHODS
FOR PROCESSING SIGNALS BETWEEN A
TESTER AND A PLURALITY OF DEVICES
UNDER TEST AT HIGH TEMPERATURES
AND WITH SINGLE TOUCHDOWN OF A
PROBE ARRAY****Publication Classification**(51) **Int. Cl.**
G01R 31/28 (2006.01)(52) **U.S. Cl.** **324/158.1**(57) **ABSTRACT**

Apparatus is for processing signals between a tester and devices under test. In one embodiment, the apparatus includes at least one multichip module. Each multichip module has a plurality of micro-electromechanical switches between a set of connectors to the tester and a set of connectors to devices under test. At least one driver is provided to operate each of the micro-electromechanical switches. A method of processing signals between a tester and devices under test is disclosed. In an embodiment, the method includes connecting the tester and the devices under test with at least one multichip module. Each of the at least one multichip module has a plurality of micro-electromechanical switches between a set of connectors to the tester and a set of connectors to the devices under test. The method includes operating each of the micro-electromechanical switches. Other embodiments are also disclosed.

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FORT COLLINS, CO 80528 (US)(21) **Appl. No.: 11/410,699**(22) **Filed: Apr. 24, 2006**

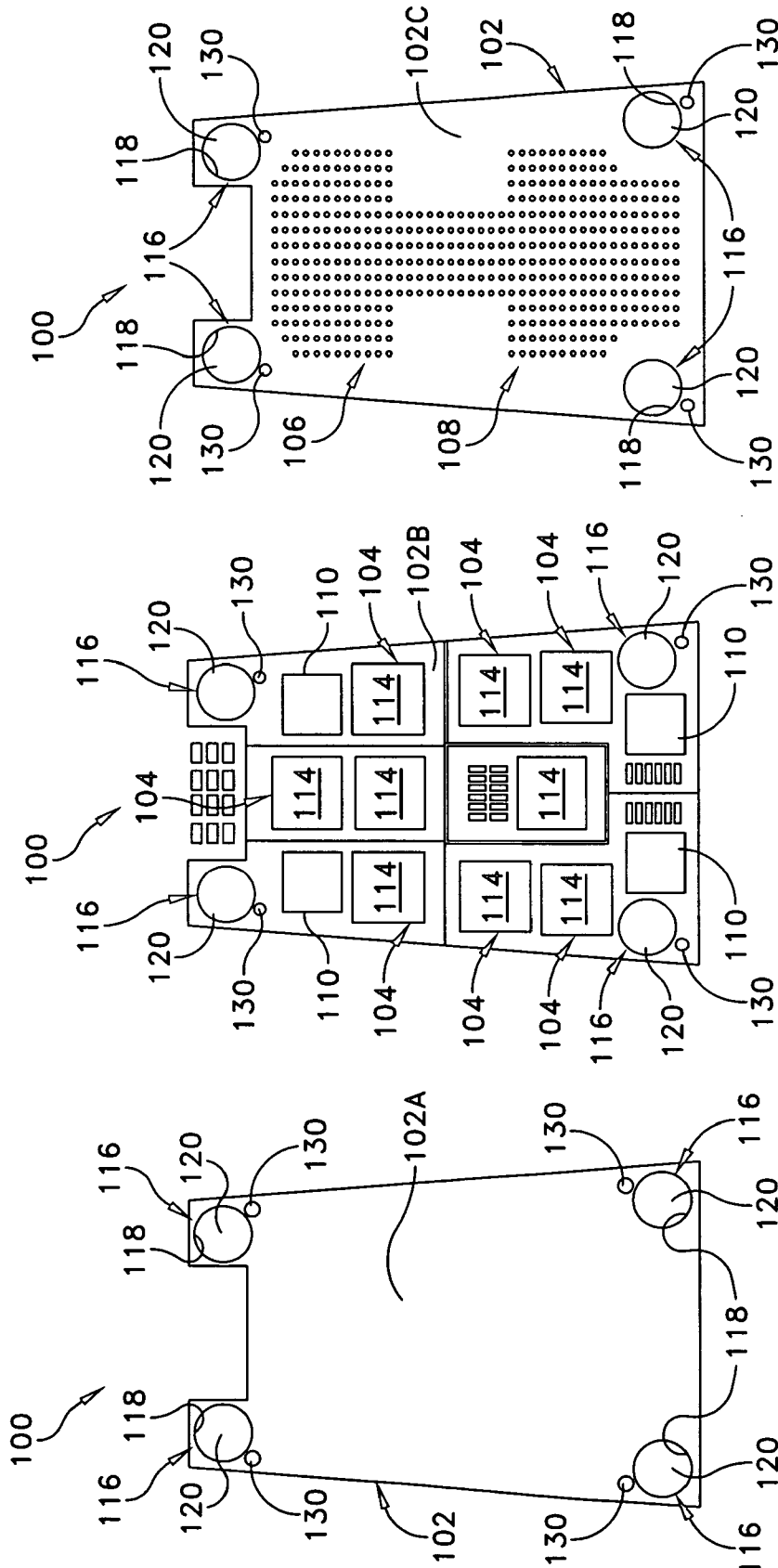


FIGURE 1

FIGURE 2

FIGURE 3

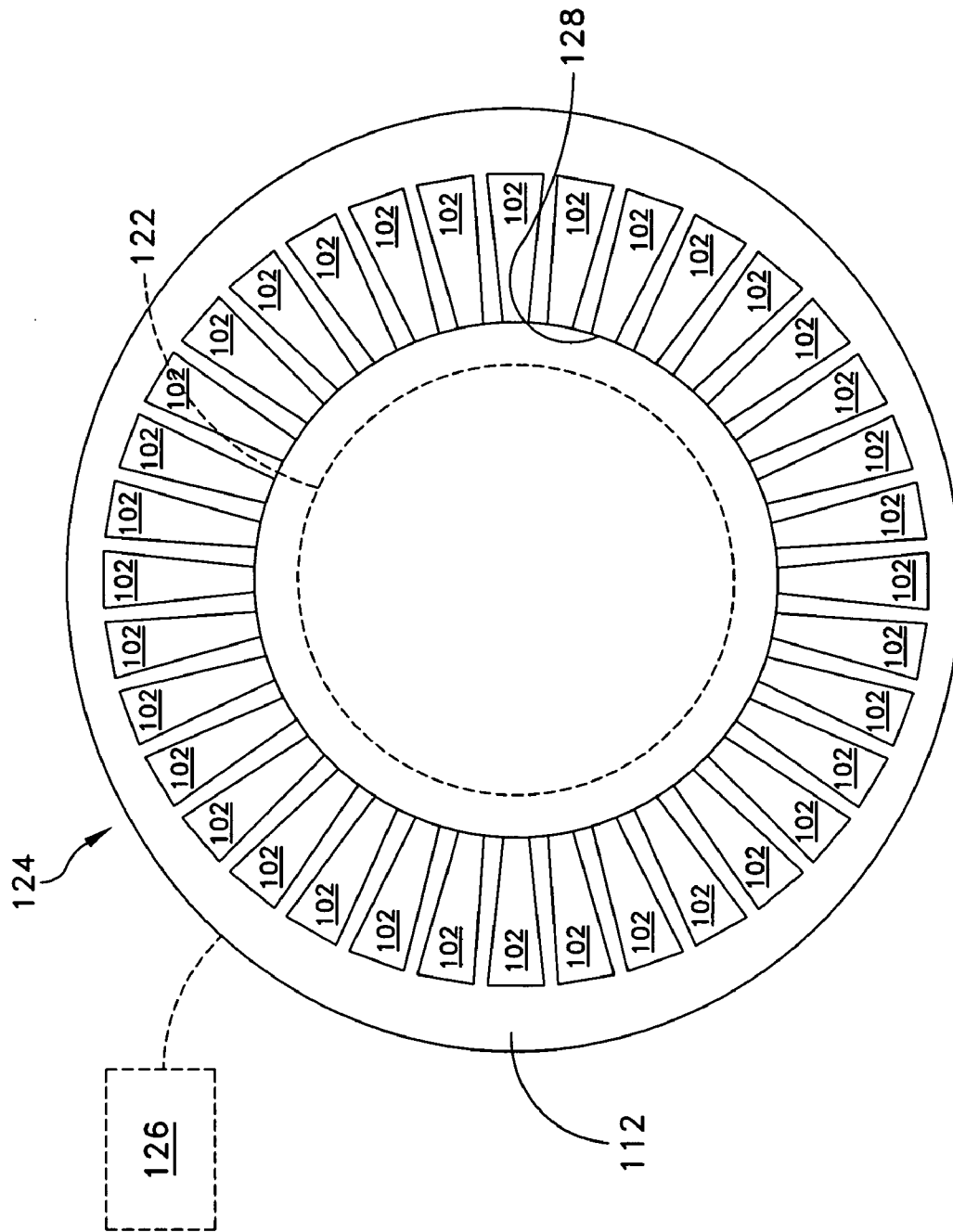


FIGURE 4

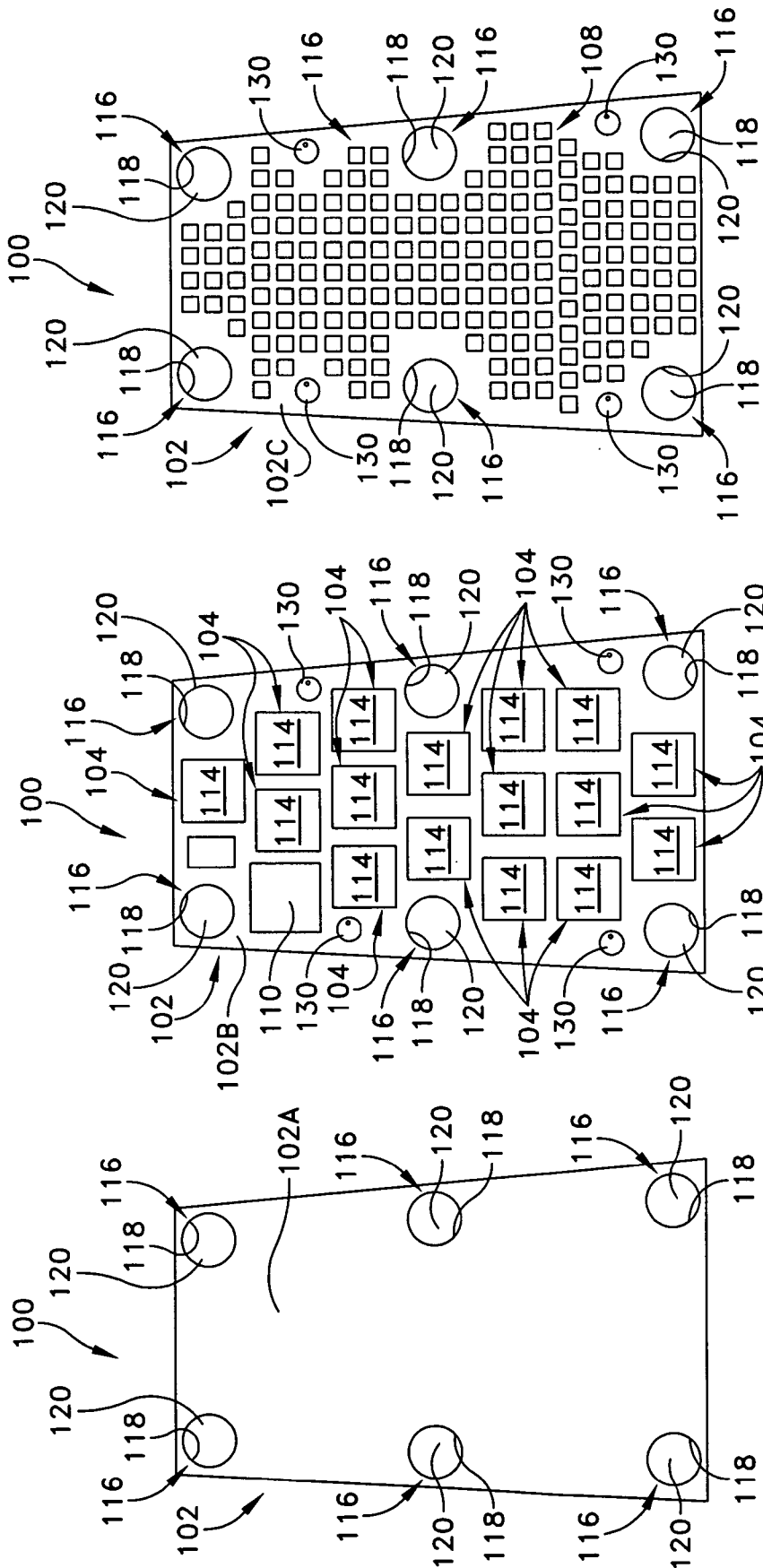


FIGURE 5

FIGURE 6

FIGURE 7

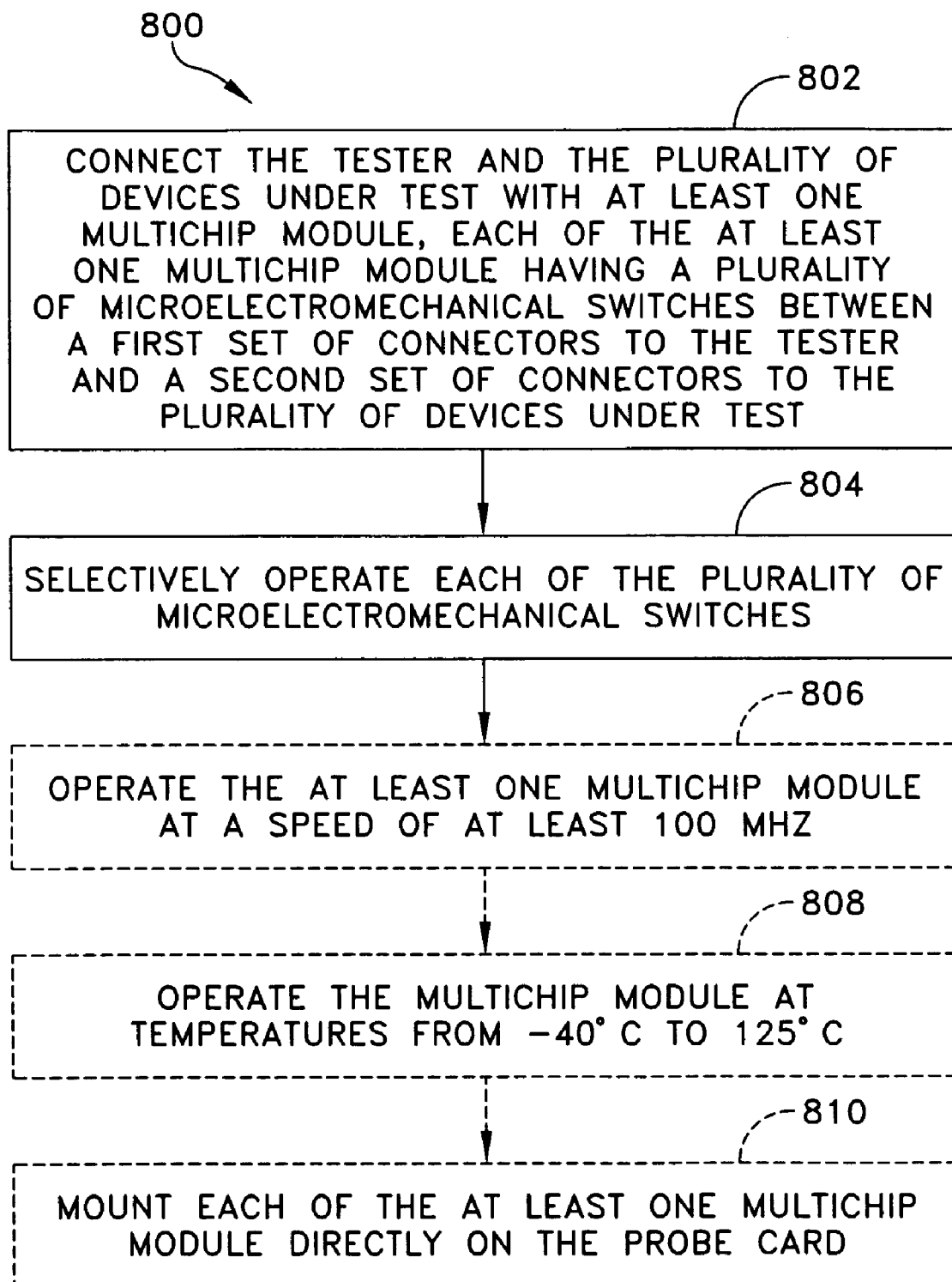


FIGURE 8

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APPARATUS, SYSTEMS AND METHODS FOR PROCESSING SIGNALS BETWEEN A TESTER AND A PLURALITY OF DEVICES UNDER TEST AT HIGH TEMPERATURES AND WITH SINGLE TOUCHDOWN OF A PROBE ARRAY

BACKGROUND

[0001] Others have developed solutions for two touch-down testing of 300 mm wafers containing many NAND dice, e.g. 432 NAND dice having 16 test sites each for a total of 6912 test sites. Generally, this type of testing utilizes mechanical relays installed in the device under test (DUT) interface of the automatic test equipment (ATE) system. These relays are typically located electrically far away from the device under test (DUT). This distance may create a large impedance mismatch when reading back from the device. In addition, the maximum data rate for testing the device may be limited to only 20 MHz.

[0002] Mechanical relays are also quite expensive. For example, the typical mechanical relays may each cost about \$8.00. This may limit the return on investment (ROI) for the customer. Mechanical relays are generally rated for about 1 to 10 million test cycles. This may create reliability issues for the customer over time. Furthermore, mechanical relays are only rated for operation up to 85° C. This allows testing of NAND devices using mechanical relays at or below 85° C.

[0003] Other solutions for multiplexing a large number of tester pin electronics (PE) by mounting a plurality of daughter boards on probe cards. This will only allow two touch-down testing of 300 mm wafers of NAND dice. This daughter card approach has limitations with respect to temperature and density. The connector limits the density of switches that can be placed on the daughter card and the active silicon switches have a temperature limitation of 85° C. when using standard grade integrated chips.

SUMMARY OF THE INVENTION

[0004] In an embodiment, there is provided apparatus for processing signals between a tester and a plurality of devices under test, the apparatus comprising at least one multichip module, each of the at least one multichip module comprising a plurality of micro-electromechanical switches between a first set of connectors to the tester and a second set of connectors to the plurality of devices under test; and at least one driver to selectively operate each of the plurality of micro-electromechanical switches.

[0005] In another embodiment, there is provided a system for testing a plurality of devices under test, the system comprising a set of tester electronics to generate signals for application to the plurality of devices under test, and to receive signals generated by the plurality of devices under test; a probe card with at least one multichip module mounted thereon, each of the at least one multichip module comprising a plurality of micro-electromechanical switches between a first set of connectors to the set of tester electronics and a second set of connectors to the plurality of devices under test, and a driver to selectively operate each of the plurality of micro-electromechanical switches; and a probe array to transmit signals between the at least one multichip module of the probe card and the plurality of devices under test.

[0006] In yet another embodiment, there is provided apparatus for processing signals between a tester and a plurality of devices under test, the apparatus comprising at least one multichip module mounted directly on a probe card and operable at a temperature of at least 125° C., and each of the at least one multichip module having a plurality of micro-electromechanical switches between a first set of connectors to the tester and a second set of connectors to the plurality of devices under test.

[0007] In still another embodiment, there is provided a method of processing signals between a tester and a plurality of devices under test, the method comprising connecting the tester and the plurality of devices under test with at least one multichip module, each of the at least one multichip module having a plurality of micro-electromechanical switches between a first set of connectors to the tester and a second set of connectors to the plurality of devices under test; and selectively operating each of the plurality of micro-electromechanical switches.

[0008] Other embodiments are also disclosed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] Illustrative embodiments of the invention are illustrated in the drawings, in which:

[0010] FIGS. 1-3 illustrate one exemplary embodiment of a multichip module for processing signals between a tester and a plurality of devices under test;

[0011] FIG. 4 illustrates a system having a probe card with a plurality of multichip modules for processing signals between a tester and a plurality of devices under test;

[0012] FIGS. 5-7 illustrate another exemplary embodiment of a multichip module for processing signals between a tester and a plurality of devices under test; and

[0013] FIG. 8 is a flow chart diagram illustrative of methods of processing signals between a tester and a plurality of devices under test.

DETAILED DESCRIPTION OF AN EMBODIMENT

[0014] Referring to FIGS. 1-7, there is shown apparatus 100 for processing signals between a tester and a plurality of devices under test. In one embodiment, apparatus 100 may include various types of multichip modules 102, which are also referred to as MCMs 102. FIGS. 1-3 illustrate one exemplary embodiment of multichip module 102. FIGS. 4-7 illustrate another exemplary embodiment of multichip module 102.

[0015] A top cover 102A of multichip module 102 is shown in FIGS. 1 and 5. A cross-sectional plan view 102B of multichip module 102 is shown in FIGS. 2 and 6. A bottom portion 102C is shown in FIGS. 3 and 6.

[0016] Referring to FIGS. 2 and 5, and each multichip module 102 may include a plurality of micro-electromechanical switches 104, which are also referred to as MEMs 104, between a first set of connectors 106 to the tester and a second set of connectors 108 to the plurality of devices under test. Each multichip module may include at least one driver 110 to selectively operate each of the plurality of micro-electromechanical switches 104.

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[0017] Looking at FIG. 4, and in an embodiment, apparatus 100 for processing signals may include a configuration in which each of multichip modules 102 are mounted directly on a probe card 112. Due to the proximity of multichip modules 102 to probe card 112 and the devices under test (not shown), one or more of multichip modules 102 may operate at a speed of at least 100 MHz. In another embodiment, one or more of multichip modules 102 may operate at a speed above 20 MHz to about 100 MHz.

[0018] In an embodiment, one or more of multichip modules 102 may operate at a temperature with a range from about -40° C. to about 125° C. In another embodiment, one or more of multichip modules 102 may operate within a temperature range from about 85° C. to about 125° C.

[0019] In one embodiment, one or more of multichip modules 102 may be rated for at least 1 billion test cycles. Multichip modules 102 may be rated for 10 billion or more test cycles. This is due, at least in part, to the micro-electromechanical switches 104 that may be used instead of other types of switches.

[0020] Referring to FIGS. 2 and 6, and in an embodiment, the plurality of micro-electromechanical switches 104 may be housed in separate MEMS dice 114. In one embodiment, each of the separate MEMS dice 114 may include eight single pole triple throw switches (FIG. 2). In another embodiment, each of the separate MEMS dice 114 may include eight single pole double throw switches (FIG. 6).

[0021] Looking at FIGS. 1-3 and 5-7, an attachment component 116 may be provided to secure one or more of multichip modules 102. In an embodiment, attachment component 116 mounts multichip module 102 to probe card 112 (FIG. 4). Attachment component 116 may include passage-ways 118 through multichip module 102 for a set of screws 120 to mount the multichip module to probe card 112 (FIG. 4).

[0022] As MEM MCM 102 may be attached to probe card 112 using screws 120 or other fasteners, a new tester does not need to be purchased from a supplier of the ATE system. A customer may simply design a probe card and attach these MEM MCMS to the probe card and install this new probe card assembly onto an existing ATE system.

[0023] Generally, MCM 102 may be very thin to allow probe card 112 together with MCMS 102 to fit into an auto loader of a prober. Many screws 120 or other fasteners may be used to attach MCM 102 to probe card 112 to prevent warping.

[0024] In an embodiment, one or more of drivers 110 may be designed to supply an electrostatic potential to selectively activate a MEMS gate associated with one or more of the plurality of micro-electromechanical switches 104. One or more of drivers 110 may be a vacuum-fluorescent display driver die 110. In one embodiment, four drivers 110 (FIG. 2) act as an algorithmic pattern generating system (APGS) and supply the electrostatic potential to four separate DUTs independently of one another. In another embodiment, one driver 110 (FIG. 6) acts as an algorithmic pattern generating system (APGS) and supplies electrostatic potential to DUTs.

[0025] In one embodiment, the second set of connectors of multichip modules 102 attach to a probe array 122. This probe array 122 may have at least 6000 probe tip needles so

as to test at least 6000 test sites of the plurality of devices under test during a single touchdown of probe array 122. For example, each multichip module 102 may test 12 DUTs, there may be 36 multichip modules in attachment to probe card 112 for a total of 432 DUTs, and there may be 16 test sites on each one of the DUTs for a total of 6912 test sites, which in turn requires 6912 probe tip needles.

[0026] Referring to FIG. 4, and in an embodiment, there is shown a system 124 for testing a plurality of devices under test. System 124 may include a set of tester electronics 126 to generate signals for application to the plurality of devices under test, and to receive signals generated by the plurality of devices under test. System 124 may include probe card 112 with at least one multichip module 102 mounted directly on probe card 112. Each of the at least one multichip module 102 may include a plurality of micro-electromechanical switches 104 between a first set of connectors to the set of tester electronics 126 and a second set of connectors to the plurality of devices under test. System may include one or more drivers 110 to selectively operate each of the plurality of micro-electromechanical switches 104. System 124 may further include probe array 122 to transmit signals between the multichip modules 102 of probe card 112 and the plurality of devices under test.

[0027] In one embodiment, probe card 112 may have 36 multichip modules 102 mounted thereon. Each of multichip modules 102 may have a plurality of MEMS dice 114 thereon. Furthermore, each one of the plurality of MEMS dice 114 may each contain a plurality of switches 104. In one embodiment, switches 104 may include single pole triple throw switches. In another embodiment, switches 104 may include single pole double throw switches.

[0028] Looking at FIG. 1, and in an embodiment, each of multichip modules 102 may have 9 MEMS dice 114 thereon. In one embodiment, each of the 9 MEMS dice 114 may have 8 MEMS switches 104. Looking at FIG. 4, and in another embodiment, each of multichip modules 102 may have 16 MEMS dice 114 thereon. In an embodiment, each of the 16 MEMS dice 114 may have 8 MEMS switches 104.

[0029] Referring to FIGS. 3 and 7, and in an embodiment, each one multichip module 104 may be housed in a standard package configuration having 780 pins which may be configured on bottom portion 102C. A portion of the 780 pins form first set of connectors 106, which may provide electrical connection to tester electronics. Another portion of the 780 pins form second set of connectors 108, which may provide electrical connection to devices under test.

[0030] Probe card 112 may have a maximum diameter of 440 millimeters. Probe card 112 may form an opening 128 for probe array 122. In an embodiment, opening 128 has a minimum diameter of 330 millimeters. Probe card 112 may contain at least 36 of multichip modules 102 mounted thereon.

[0031] In an embodiment, probe array 112 may have at least 6000 probe tip needles so as to test at least 6000 test sites of the plurality of devices under test during a single touchdown of probe array 112.

[0032] In an embodiment, system 124 enables one touchdown testing of 300 mm wafers containing NAND devices to be tested up to 100 MHz by mounting micro-electromechanical multichip modules 102 very close to the DUTs.

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This one touchdown testing cannot be achieved by using mechanical relays or active silicon devices mounted on daughter boards. Daughter boards mounted on the probe cannot achieve the required density of switches because of the space required for connectors. Mechanical relays, which are mounted far from the DUTs, are generally limited to about 20 MHz and cannot achieve a data rate near 100 MHz.

[0033] For example, and looking at FIGS. 1-3, to achieve a desired data rate of about 20 MHz to about 100 MHz, 72 single-pole, triple-throw (SPTT) MEM switches **104** and four vacuum-florescent display driver dice (VFD) **110** may be integrated into one 780 pin multichip module (MCM) **102**. This MCM **102** may measure 26 mm×55 mm×34 mm×55 mm (see FIG. 1).

[0034] In one embodiment, and looking at FIGS. 5-7, to achieve a desired data rate of about 20 MHz to about 100 MHz, 128 single-pole, double-throw (SPDT) MEM switches **104** and one vacuum-florescent display driver die (VFD) **110** with 32 outputs may be integrated into one 780 pin multichip module (MCM) **102**. This MCM **102** may measure 26 mm×55 mm×34 mm×55 mm (see FIG. 5).

[0035] MEM MCMs **102** may be fabricated quite inexpensively. For example, an MCM package containing 128 SPDT switches with only 780 pins may cost about \$300 per package. This drastically improves the return on investment (ROI) for the customer.

[0036] As discussed above, mechanical relays are generally rated a maximum testing temperature of 85° C., which is due to the moving parts inside the relay housing. Implementations using active silicon devices are also typically rated for a maximum testing temperature of 85° C. Using either of these, i.e. mechanical relays or daughter boards with active silicon, NAND devices may only be tested up to 85° C. However, using system **100**, NAND devices may be tested at temperatures ranging from -40° C. to 125° C. with one or more of MEM MCMs **102**.

[0037] MEM MCMs **102** are generally mounted very close to the DUTs so as to increase the maximum data rate for testing NAND devices from 20 MHz to 100 MHz, and also to enable testing of the entire 300 mm wafer with one touchdown.

[0038] Utilizing MEM MCMs **102** instead of mechanical relays is also more cost effective and more reliable. A typical mechanical relay is rated for 1-10 million cycles. A typical MEM MCM **102** may be rated for 1-10 billion cycles. Using daughter boards limits the density of switches that can be mounted on the probe card due to the space required for connectors.

[0039] Multichip modules **102** are generally capable of much higher densities than daughter cards. Mounting multichip modules **102** onto probe card **112** enables the customer to double the pin count of the test system when testing NAND devices without buying a new ATE system.

[0040] Using the Agilent V5400 test system, 16 NAND devices with 36 test sites each may be tested. Each MEMs dice may have 8 SPDT switches. The electrostatic potential required to activate the MEMs gate will be supplied by a vacuum-florescent display driver die **110** located inside the MCM package **102**. MCM substrate **102B** may be a blind and buried via substrate made of NELCO 4000-13 Si, which

is a typical MCM substrate. Connectors **106** and connectors **108** may include, but are not limited to pins. Such pins of the package may include Be—Cu springs that are attached with silver epoxy to the bottom of the NELCO 4000-13 Si substrate. MEMs **104** and single VFD **110** may be located inside MCM **102** and may be wired bond or soldered to the substrate.

[0041] In an embodiment, MCMs **102** may be reusable. MCMs **102** can be transferred from one probe card to another when the probe card becomes damaged or is simply obsolete due to a change in die size or layout on the wafers.

[0042] Alignment pins **130** may be provided to align MCM **102** to probe card **112**.

[0043] Looking now at FIG. 8, and in an embodiment, there is provided a method **800** of processing signals between a tester and a plurality of devices under test. Method **800** may include connecting **802** the tester and the plurality of devices under test with at least one multichip module, each of the at least one multichip module having a plurality of micro-electromechanical switches between a first set of connectors to the tester and a second set of connectors to the plurality of devices under test. Method **800** may include selectively operating **804** each of the plurality of micro-electromechanical switches.

[0044] In one embodiment, method **800** may further include operating **806** the at least one multichip module at a speed of at least 100 MHz. In an embodiment, method **800** may include operating **808** the multichip module at temperatures from -40° C. to 125° C.

[0045] Method **800** may include mounting **810** each of the at least one multichip module directly on the probe card.

1. Apparatus for processing signals between a tester and a plurality of devices under test, the apparatus comprising:

at least one multichip module, each of the at least one multichip module comprising:

a plurality of micro-electromechanical switches between a first set of connectors to the tester and a second set of connectors to the plurality of devices under test; and

at least one driver to selectively operate each of the plurality of micro-electromechanical switches.

2. Apparatus in accordance with claim 1, further comprising a probe card on which each one of the at least one multichip module is directly mounted.

3. Apparatus in accordance with claim 1, further comprising a plurality of MEMs dice on which the plurality of micro-electromechanical switches are formed.

4. Apparatus in accordance with claim 1, wherein the separate MEMs dice each include eight single pole triple throw switches.

5. Apparatus in accordance with claim 1, further comprising an attachment component for each one of the at least one multichip module, and wherein the attachment component mounts the multichip module to a probe card.

6. Apparatus in accordance with claim 5, wherein the attachment component includes passageways through the multichip module for a set of screws to mount the multichip module to the probe card.

7. Apparatus in accordance with claim 1, wherein the driver is designed to supply an electrostatic potential to

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activate a MEMS gate associated with each of the plurality of micro-electromechanical switches.

8. Apparatus in accordance with claim 1, wherein the at least one driver comprises a vacuum-florescent display driver dice.

9. A system for processing signals between a tester and a plurality of devices under test, the system comprising:

at least one multichip module mounted directly on a probe card and operable at a temperature of at least 125° C., and each of the at least one multichip module having a plurality of micro-electromechanical switches between a first set of connectors to the tester and a second set of connectors to the plurality of devices under test.

10. A system in accordance with claim 9, wherein the second set of connectors attach to a probe array having at least 6000 probe tip needles so as to test at least 6000 test sites of the plurality of devices under test during a single touchdown of the probe array.

11. A system for testing a plurality of devices under test, the system comprising:

a set of tester electronics to generate signals for application to the plurality of devices under test, and to receive signals generated by the plurality of devices under test;

a probe card with at least one multichip module mounted thereon, each of the at least one multichip module comprising a plurality of micro-electromechanical switches between a first set of connectors to the set of tester electronics and a second set of connectors to the plurality of devices under test, and a driver to selectively operate each of the plurality of micro-electromechanical switches; and

a probe array to transmit signals between the at least one multichip module of the probe card and the plurality of devices under test.

12. A system in accordance with claim 11, wherein each of the at least one multichip modules has a plurality of MEMS dice thereon.

13. A system in accordance with claim 11, wherein each one of the plurality of MEMS dice each contain a plurality of micro-electromechanical switches.

14. A system in accordance with claim 13, wherein the switches are single pole triple throw switches.

15. A system in accordance with claim 13, wherein the switches are single pole double throw switches.

16. A system in accordance with claim 11, wherein the probe card has a maximum diameter of 440 millimeters.

17. A system in accordance with claim 16, wherein the probe card forms an opening for the probe array, and the opening has a minimum diameter of 330 millimeters.

18. A system in accordance with claim 11, wherein the probe array has at least 6000 probe tip needles so as to test at least 6000 test sites of the plurality of devices under test during a single touchdown of the probe array.

19. A method of processing signals between a tester and a plurality of devices under test, the method comprising:

connecting the tester and the plurality of devices under test with at least one multichip module, each of the at least one multichip module having a plurality of micro-electromechanical switches between a first set of connectors to the tester and a second set of connectors to the plurality of devices under test; and

selectively operating each of the plurality of micro-electromechanical switches to process the signals between individual ones of the first set of connectors to the tester and selected multiple ones of the second set of connectors to the Plurality of devices under test.

20. A method in accordance with claim 19, further comprising operating the at least one multichip module at a speed of at least 100 MHz.

21. A method in accordance with claim 19, further comprising operating the multichip module at a temperature of at least 125° C.

22. A method in accordance with claim 19, further comprising mounting each of the at least one multichip module directly on the probe card.

23. A method in accordance with claim 19, further comprising mounting each of the at least one multichip module directly on the probe card, operating the multichip module at a temperature of at least 125° C., and operating the at least one multichip module at a speed of at least 100 MHz.

* * * * *



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Transmitted herewith for filing under 37 CFR 1.53(b) is a(n): ☒ Utility ☐ Design
☒ Original patent application,
☐ Continuation-in-part

INVENTOR(S): Romi Mayder, et al.

TITLE: APPARATUS, SYSTEMS AND METHODS FOR PROCESSING SIGNALS BETWEEN A TESTER AND A
PLURALITY OF DEVICES UNDER TEST AT HIGH TEMPERATURES AND WITH SINGLE TOUCHDOWN
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Enclosed are:

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INDEPENDENT CLAIMS	4 - 3	1	X \$200	\$ 200
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TOTAL SHEETS OF SPEC AND DWGS	24 - 100	0	X \$250/50	\$ 0
BASIC FEE: Design (\$350.00); Utility (\$1000.00)				\$ 1,000
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Respectfully submitted,

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By:

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04/24/06

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Romi Mayder, et al.

Serial No.: Not Yet Assigned

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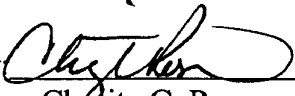
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I hereby certify that the following attached documents:

- Patent Application Transmittal Letter (in duplicate);
- Signed Declaration and Power of Attorney (2 sheets);
- Specification (20 pages including 14 pages of specification, 5 pages of claims and 1 page abstract);
- 4 sheets of Formal Drawings (Illustrating Figs. 1-8); and
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(1) FOR	(2) NUMBER FILED	(3) NUMBER EXTRA	(4) RATE	(5) TOTALS
TOTAL CLAIMS	23 - 20	3	X \$ 50	\$ 150
INDEPENDENT CLAIMS	4 - 3	1	X \$200	\$ 200
ANY MULTIPLE DEPENDENT CLAIMS	0		\$360	\$ 0
TOTAL SHEETS OF SPEC AND DWGS	24 - 100	0	X \$250/50	\$ 0
BASIC FEE: Design (\$350.00); Utility (\$1000.00)				\$ 1,000
TOTAL FILING FEE				\$ 1,350
OTHER FEES				\$ 0
TOTAL CHARGES TO DEPOSIT ACCOUNT				\$ 1,350

Charge \$1,350 to Deposit Account 50-1078. At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account 50-1078 pursuant to 37 CFR 1.25. Additionally please charge any fees to Deposit Account 50-1078 under 37 CFR 1.16, 1.17, 1.19, 1.20 and 1.21. A duplicate copy of this sheet is enclosed.

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I hereby certify that this is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria VA 22313-1450.

Typed Name: Chasity C. Rossum

Signature:

Respectfully submitted,

Romi Mayder, et al.

By:

James A. Sheridan
Attorney/Agent for Applicant(s)

04/24/06

Reg. No. 43,114

Date: April 24, 2006

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:

Romi Mayder, et al.

Serial No.: Not Yet Assigned

Filing Date: April 24, 2006

Docket No.: 10060220-1

Confirmation No.: Not Yet Assigned

Examiner: Not Yet Assigned

Group Art Unit: Not Yet Assigned

For: APPARATUS, SYSTEMS AND METHODS FOR PROCESSING SIGNALS BETWEEN A TESTER AND A PLURALITY OF DEVICES UNDER TEST AT HIGH TEMPERATURES AND WITH SINGLE TOUCHDOWN OF A PROBE ARRAY

CERTIFICATE OF EXPRESS MAILING

I hereby certify that the following attached documents:

- Patent Application Transmittal Letter (in duplicate);
- Signed Declaration and Power of Attorney (2 sheets);
- Specification (20 pages including 14 pages of specification, 5 pages of claims and 1 page abstract);
- 4 sheets of Formal Drawings (Illustrating Figs. 1-8); and
- Postcards for return by the United States Patent and Trademark Office,

are all being deposited with the United States Postal Service addressed to the Mail Stop Patent Application, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, via Express Mail No. EV554755343US, on this 24th day of April, 2006.

By



Chasity C. Rossum
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303-291-3200

SPECIFICATION

TO WHOM IT MAY CONCERN:

Be it known that we, with names, residences, and citizenships listed below, have invented the inventions described in the following specification entitled:

**APPARATUS, SYSTEMS AND METHODS FOR PROCESSING SIGNALS
BETWEEN A TESTER AND A PLURALITY OF DEVICES UNDER TEST AT HIGH
TEMPERATURES AND WITH SINGLE TOUCHDOWN OF A PROBE ARRAY**

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**APPARATUS, SYSTEMS AND METHODS FOR PROCESSING SIGNALS
BETWEEN A TESTER AND A PLURALITY OF DEVICES UNDER TEST AT HIGH
TEMPERATURES AND WITH SINGLE TOUCHDOWN OF A PROBE ARRAY**

Background

[0001] Others have developed solutions for two touchdown testing of 300 mm wafers containing many NAND dice, e.g. 432 NAND dice having 16 test sites each for a total of 6912 test sites. Generally, this type of testing utilizes mechanical relays installed in the device under test (DUT) interface of the automatic test equipment (ATE) system. These relays are typically located electrically far away from the device under test (DUT). This distance may create a large impedance mismatch when reading back from the device. In addition, the maximum data rate for testing the device may be limited to only 20 MHz.

[0002] Mechanical relays are also quite expensive. For example, the typical mechanical relays may each cost about \$8.00. This may limit the return on investment (ROI) for the customer. Mechanical relays are generally rated for about 1 to 10 million test cycles. This may create reliability issues for the customer over time. Furthermore, mechanical relays are only rated for operation up to 85° C. This allows testing of NAND devices using mechanical relays at or below 85° C.

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[0003] Other solutions for multiplexing a large number of tester pin electronics (PE) by mounting a plurality of daughter boards on probe cards. This will only allow two touchdown testing of 300 mm wafers of NAND dice. This daughter card approach has limitations with respect to temperature and density. The connector limits the density of switches that can be placed on the daughter card and the active silicon switches have a temperature limitation of 85° C when using standard grade integrated chips.

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Summary of the Invention

[0004] In an embodiment, there is provided apparatus for processing signals between a tester and a plurality of devices under test, the apparatus comprising at least one multichip module, each of the at least one multichip module comprising a plurality of micro-electromechanical switches between a first set of connectors to the tester and a second set of connectors to the plurality of devices under test; and at least one driver to selectively operate each of the plurality of micro-electromechanical switches.

[0005] In another embodiment, there is provided a system for testing a plurality of devices under test, the system comprising a set of tester electronics to generate signals for application to the plurality of devices under test, and to receive signals generated by the plurality of devices under test; a probe card with at least one multichip module mounted thereon, each of the at least one multichip module comprising a plurality of micro-electromechanical switches between a first set of connectors to the set of tester electronics and a second set of connectors to the plurality of devices under test, and a driver to selectively operate each of the plurality of micro-electromechanical switches; and a probe array to transmit signals between the at least one multichip module of the probe card and the plurality of devices under test.

[0006] In yet another embodiment, there is provided apparatus for processing signals between a tester and a plurality of devices under test, the apparatus comprising at least one multichip module mounted directly on a probe card and

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operable at a temperature of at least 125° C, and each of the at least one multichip module having a plurality of micro-electromechanical switches between a first set of connectors to the tester and a second set of connectors to the plurality of devices under test.

[0007] In still another embodiment, there is provided a method of processing signals between a tester and a plurality of devices under test, the method comprising connecting the tester and the plurality of devices under test with at least one multichip module, each of the at least one multichip module having a plurality of micro-electromechanical switches between a first set of connectors to the tester and a second set of connectors to the plurality of devices under test; and selectively operating each of the plurality of micro-electromechanical switches.

[0008] Other embodiments are also disclosed.

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Brief Description of the Drawings

[0009] Illustrative embodiments of the invention are illustrated in the drawings, in which:

[0010] FIGURES 1-3 illustrate one exemplary embodiment of a multichip module for processing signals between a tester and a plurality of devices under test;

[0011] FIGURE 4 illustrates a system having a probe card with a plurality of multichip modules for processing signals between a tester and a plurality of devices under test ;

[0012] FIGURES 5-7 illustrate another exemplary embodiment of a multichip module for processing signals between a tester and a plurality of devices under test; and

[0013] FIGURE 8 is a flow chart diagram illustrative of methods of processing signals between a tester and a plurality of devices under test.

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Detailed Description of an Embodiment

[0014] Referring to FIGURES 1-7, there is shown apparatus 100 for processing signals between a tester and a plurality of devices under test. In one embodiment, apparatus 100 may include various types of multichip modules 102, which are also referred to as MCMs 102. FIGURES 1-3 illustrate one exemplary embodiment of multichip module 102. FIGURES 4-7 illustrate another exemplary embodiment of multichip module 102.

[0015] A top cover 102A of multichip module 102 is shown in FIGURES 1 and 5. A cross-sectional plan view 102B of multichip module 102 is shown in FIGURES 2 and 6. A bottom portion 102C is shown in FIGURES 3 and 6.

[0016] Referring to FIGURES 2 and 5, and each multichip module 102 may include a plurality of micro-electromechanical switches 104, which are also referred to as MEMs 104, between a first set of connectors 106 to the tester and a second set of connectors 108 to the plurality of devices under test. Each multichip module may include at least one driver 110 to selectively operate each of the plurality of micro-electromechanical switches 104.

[0017] Looking at FIGURE 4, and in an embodiment, apparatus 100 for processing signals may include a configuration in which each of multichip modules 102 are mounted directly on a probe card 112. Due to the proximity of multichip modules 102 to probe card 112 and the devices under test (not shown), one or more of multichip modules 102 may operate at a speed of at least 100 MHz. In another embodiment, one or more of multichip modules 102 may operate at a

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speed above 20 MHz to about 100 MHz.

[0018] In an embodiment, one or more of multichip modules 102 may operate at a temperature with a range from about -40° C to about 125° C. In another embodiment, one or more of multichip modules 102 may operate within a temperature range from about 85° C to about 125° C.

[0019] In one embodiment, one or more of multichip modules 102 may be rated for at least 1 billion test cycles. Multichip modules 102 may be rated for 10 billion or more test cycles. This is due, at least in part, to the micro-electromechanical switches 104 that may be used instead of other types of switches.

[0020] Referring to FIGURES 2 and 6, and in an embodiment, the plurality of micro-electromechanical switches 104 may be housed in separate MEMs dice 114. In one embodiment, each of the separate MEMs dice 114 may include eight single pole triple throw switches (FIGURE 2). In another embodiment, each of the separate MEMs dice 114 may include eight single pole double throw switches (FIGURE 6).

[0021] Looking at FIGURES 1-3 and 5-7, an attachment component 116 may be provided to secure one or more of multichip modules 102. In an embodiment, attachment component 116 mounts multichip module 102 to probe card 112 (FIGURE 4). Attachment component 116 may include passageways 118 through multichip module 102 for a set of screws 120 to mount the multichip module to probe card 112 (FIGURE 4).

[0022] As MEM MCM 102 may be attached to probe card 112 using screws 120 or other fasteners, a new tester does not need to be purchased from a supplier of

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the ATE system. A customer may simply design a probe card and attach these MEM MCMs to the probe card and install this new probe card assembly onto an existing ATE system.

[0023] Generally, MCM 102 may be very thin to allow probe card 112 together with MCMs 102 to fit into an auto loader of a prober. Many screws 120 or other fasteners may be used to attach MCM 102 to probe card 112 to prevent warping.

[0024] In an embodiment, one or more of drivers 110 may be designed to supply an electrostatic potential to selectively activate a MEMs gate associated with one or more of the plurality of micro-electromechanical switches 104. One or more of drivers 110 may be a vacuum-florescent display driver die 110. In one embodiment, four drivers 110 (FIGURE 2) act as an algorithmic pattern generating system (APGS) and supply the electrostatic potential to four separate DUTs independently of one another. In another embodiment, one driver 110 (FIGURE 6) acts as an algorithmic pattern generating system (APGS) and supplies electrostatic potential to DUTs.

[0025] In one embodiment, the second set of connectors of multichip modules 102 attach to a probe array 122. This probe array 122 may have at least 6000 probe tip needles so as to test at least 6000 test sites of the plurality of devices under test during a single touchdown of probe array 122. For example, each multichip module 102 may test 12 DUTs, there may be 36 multichip modules in attachment to probe card 112 for a total of 432 DUTs, and there may be 16 test sites on each one of the DUTs for a total of 6912 test sites, which in turn requires 6912 probe tip needles.

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[0026] Referring to FIGURE 4, and in an embodiment, there is shown a system 124 for testing a plurality of devices under test. System 124 may include a set of tester electronics 126 to generate signals for application to the plurality of devices under test, and to receive signals generated by the plurality of devices under test. System 124 may include probe card 112 with at least one multichip module 102 mounted directly on probe card 112. Each of the at least one multichip module 102 may include a plurality of micro-electromechanical switches 104 between a first set of connectors to the set of tester electronics 126 and a second set of connectors to the plurality of devices under test. System may include one or more drivers 110 to selectively operate each of the plurality of micro-electromechanical switches 104. System 124 may further include probe array 122 to transmit signals between the multichip modules 102 of probe card 112 and the plurality of devices under test.

[0027] In one embodiment, probe card 112 may have 36 multichip modules 102 mounted thereon. Each of multichip modules 102 may have a plurality of MEMS dice 114 thereon. Furthermore, each one of the plurality of MEMS dice 114 may each contain a plurality of switches 104. In one embodiment, switches 104 may include single pole triple throw switches. In another embodiment, switches 104 may include single pole double throw switches.

[0028] Looking at FIGURE 1, and in an embodiment, each of multichip modules 102 may have 9 MEMS dice 114 thereon. In one embodiment, each of the 9 MEMS dice 114 may have 8 MEMS switches 104. Looking at FIGURE 4, and in another embodiment, each of multichip modules 102 may have 16 MEMS dice 114 thereon. In an embodiment, each of the 16 MEMS dice 114 may have 8 MEMS switches

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104.

[0029] Referring to FIGURES 3 and 7, and in an embodiment, each one multichip module 104 may be housed in a standard package configuration having 780 pins which may be configured on bottom portion 102C. A portion of the 780 pins form first set of connectors 106, which may provide electrical connection to tester electronics. Another portion of the 780 pins form second set of connectors 108, which may provide electrical connection to devices under test.

[0030] Probe card 112 may have a maximum diameter of 440 millimeters. Probe card 112 may form an opening 128 for probe array 122. In an embodiment, opening 128 has a minimum diameter of 330 millimeters. Probe card 112 may contains at least 36 of multichip modules 102 mounted thereon.

[0031] In an embodiment, probe array 112 may have at least 6000 probe tip needles so as to test at least 6000 test sites of the plurality of devices under test during a single touchdown of probe array 112.

[0032] In an embodiment, system 124 enables one touchdown testing of 300 mm wafers containing NAND devices to be tested up to 100 MHz by mounting micro-electromechanical multichip modules 102 very close to the DUTs. This one touchdown testing cannot be achieved by using mechanical relays or active silicon devices mounted on daughter boards. Daughter boards mounted on the probe cannot achieve the required density of switches because of the space required for connectors. Mechanical relays, which are mounted far from the DUTs, are generally limited to about 20 MHz and cannot achieve a data rate near 100 MHz.

[0033] For example, and looking at FIGURES 1-3, to achieve a desired data rate

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of about 20 MHz to about 100 MHz, 72 single-pole, triple-throw (SPTT) MEM switches 104 and four vacuum-florescent display driver dice (VFD) 110 may be integrated into one 780 pin multichip module (MCM) 102. This MCM 102 may measure 26 mm x 55 mm x 34 mm x 55 mm (see FIGURE 1).

[0034] In one embodiment, and looking at FIGURES 5-7, to achieve a desired data rate of about 20 MHz to about 100 MHz, 128 single-pole, double-throw (SPDT) MEM switches 104 and one vacuum-florescent display driver die (VFD) 110 with 32 outputs may be integrated into one 780 pin multichip module (MCM) 102. This MCM 102 may measure 26 mm x 55 mm x 34 mm x 55 mm (see FIGURE 5).

[0035] MEM MCMs 102 may be fabricated quite inexpensively. For example, an MCM package containing 128 SPDT switches with only 780 pins may cost about \$300 per package. This drastically improves the return on investment (ROI) for the customer.

[0036] As discussed above, mechanical relays are generally rated a maximum testing temperature of 85° C, which is due to the moving parts inside the relay housing. Implementations using active silicon devices are also typically rated for a maximum testing temperature of 85° C. Using either of these, i.e. mechanical relays or daughter boards with active silicon, NAND devices may only be tested up to 85° C. However, using system 100, NAND devices may be tested at temperatures ranging from -40° C to 125° C with one or more of MEM MCMs 102.

[0037] MEM MCMs 102 are generally mounted very close to the DUTs so as to increase the maximum data rate for testing NAND devices from 20 MHz to 100 MHz, and also to enable testing of the entire 300 mm wafer with one touchdown.

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[0038] Utilizing MEM MCMs 102 instead of mechanical relays is also more cost effective and more reliable. A typical mechanical relay is rated for 1-10 million cycles. A typical MEM MCM 102 may be rated for 1-10 billion cycles. Using daughter boards limits the density of switches that can be mounted on the probe card due to the space required for connectors.

[0039] Multichip modules 102 are generally capable of much higher densities than daughter cards. Mounting multichip modules 102 onto probe card 112 enables the customer to double the pin count of the test system when testing NAND devices without buying a new ATE system.

[0040] Using the Agilent V5400 test system, 16 NAND devices with 36 test sites each may be tested. Each MEMs dice may have 8 SPDT switches. The electrostatic potential required to activate the MEMs gate will be supplied by a vacuum-florescent display driver die 110 located inside the MCM package 102. MCM substrate 102B may be a blind and buried via substrate made of NELCO 4000-13 Si, which is a typical MCM substrate. Connectors 106 and connectors 108 may include, but are not limited to pins. Such pins of the package may include Be-Cu springs that are attached with silver epoxy to the bottom of the NELCO 4000-13 Si substrate. MEMs 104 and single VFD 110 may be located inside MCM 102 and may be wired bond or soldered to the substrate.

[0041] In an embodiment, MCMs 102 may be reusable. MCMs 102 can be transferred from one probe card to another when the probe card becomes damaged or is simply obsolete due to a change in die size or layout on the wafers.

[0042] Alignment pins 130 may be provided to align MCM 102 to probe card

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112.

[0043] Looking now at FIGURE 8, and in an embodiment, there is provided a method 800 of processing signals between a tester and a plurality of devices under test. Method 800 may include connecting 802 the tester and the plurality of devices under test with at least one multichip module, each of the at least one multichip module having a plurality of micro-electromechanical switches between a first set of connectors to the tester and a second set of connectors to the plurality of devices under test. Method 800 may include selectively operating 804 each of the plurality of micro-electromechanical switches.

[0044] In one embodiment, method 800 may further include operating 806 the at least one multichip module at a speed of at least 100 MHz. In an embodiment, method 800 may include operating 808 the multichip module at temperatures from -40° C to 125° C.

[0045] Method 800 may include mounting 810 each of the at least one multichip module directly on the probe card.

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WHAT IS CLAIMED IS:

1. Apparatus for processing signals between a tester and a plurality of devices under test, the apparatus comprising:

at least one multichip module, each of the at least one multichip module comprising:

a plurality of micro-electromechanical switches between a first set of connectors to the tester and a second set of connectors to the plurality of devices under test; and

at least one driver to selectively operate each of the plurality of micro-electromechanical switches.

2. Apparatus in accordance with claim 1, further comprising a probe card on which each one of the at least one multichip module is directly mounted.

3. Apparatus in accordance with claim 1, further comprising a plurality of MEMs dice on which the plurality of micro-electromechanical switches are formed.

4. Apparatus in accordance with claim 1, wherein the separate MEMs dice each include eight single pole triple throw switches.

5. Apparatus in accordance with claim 1, further comprising an attachment component for each one of the at least one multichip module, and wherein the

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attachment component mounts the multichip module to a probe card.

6. Apparatus in accordance with claim 5, wherein the attachment component includes passageways through the multichip module for a set of screws to mount the multichip module to the probe card.

7. Apparatus in accordance with claim 1, wherein the driver is designed to supply an electrostatic potential to activate a MEMs gate associated with each of the plurality of micro-electromechanical switches.

8. Apparatus in accordance with claim 1, wherein the at least one driver comprises a vacuum-florescent display driver dice.

9. A system for processing signals between a tester and a plurality of devices under test, the system comprising:

at least one multichip module mounted directly on a probe card and operable at a temperature of at least 125° C, and each of the at least one multichip module having a plurality of micro-electromechanical switches between a first set of connectors to the tester and a second set of connectors to the plurality of devices under test.

10. A system in accordance with claim 9, wherein the second set of connectors attach to a probe array having at least 6000 probe tip needles so as to

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test at least 6000 test sites of the plurality of devices under test during a single touchdown of the probe array.

11. A system for testing a plurality of devices under test, the system comprising:

a set of tester electronics to generate signals for application to the plurality of devices under test, and to receive signals generated by the plurality of devices under test;

a probe card with at least one multichip module mounted thereon, each of the at least one multichip module comprising a plurality of micro-electromechanical switches between a first set of connectors to the set of tester electronics and a second set of connectors to the plurality of devices under test, and a driver to selectively operate each of the plurality of micro-electromechanical switches; and

a probe array to transmit signals between the at least one multichip module of the probe card and the plurality of devices under test.

12. A system in accordance with claim 11, wherein each of the at least one multichip modules has a plurality of MEMS dice thereon.

13. A system in accordance with claim 11, wherein each one of the plurality of MEMS dice each contain a plurality of micro-electromechanical switches.

14. A system in accordance with claim 13, wherein the switches are single

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pole triple throw switches.

15. A system in accordance with claim 13, wherein the switches are single pole double throw switches.

16. A system in accordance with claim 11, wherein the probe card has a maximum diameter of 440 millimeters.

17. A system in accordance with claim 16, wherein the probe card forms an opening for the probe array, and the opening has a minimum diameter of 330 millimeters.

18. A system in accordance with claim 11, wherein the probe array has at least 6000 probe tip needles so as to test at least 6000 test sites of the plurality of devices under test during a single touchdown of the probe array.

19. A method of processing signals between a tester and a plurality of devices under test, the method comprising:

connecting the tester and the plurality of devices under test with at least one multichip module, each of the at least one multichip module having a plurality of micro-electromechanical switches between a first set of connectors to the tester and a second set of connectors to the plurality of devices under test; and

selectively operating each of the plurality of micro-electromechanical

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switches.

20. A method in accordance with claim 19, further comprising operating the at least one multichip module at a speed of at least 100 MHz.

21. A method in accordance with claim 19, further comprising operating the multichip module at a temperature of at least 125° C.

22. A method in accordance with claim 19, further comprising mounting each of the at least one multichip module directly on the probe card.

23. A method in accordance with claim 19, further comprising mounting each of the at least one multichip module directly on the probe card, operating the multichip module at a temperature of at least 125° C, and operating the at least one multichip module at a speed of at least 100 MHz.

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Abstract

Apparatus is for processing signals between a tester and devices under test. In one embodiment, the apparatus includes at least one multichip module. Each multichip module has a plurality of micro-electromechanical switches between a set of connectors to the tester and a set of connectors to devices under test. At least one driver is provided to operate each of the micro-electromechanical switches. A method of processing signals between a tester and devices under test is disclosed.

In an embodiment, the method includes connecting the tester and the devices under test with at least one multichip module. Each of the at least one multichip module has a plurality of micro-electromechanical switches between a set of connectors to the tester and a set of connectors to the devices under test. The method includes operating each of the micro-electromechanical switches. Other embodiments are also disclosed.

"APPARATUS, SYSTEMS AND METHODS FOR PROCESSING SIGNALS BETWEEN A TESTER AND A PLURALITY OF DEVICES UNDER TEST AT HIGH TEMPERATURES AND WITH SINGLE TOUCHDOWN OF A PROBE ARRAY"

Inventors: Romi Mayder, et al.
Docket No.: 10060220-1

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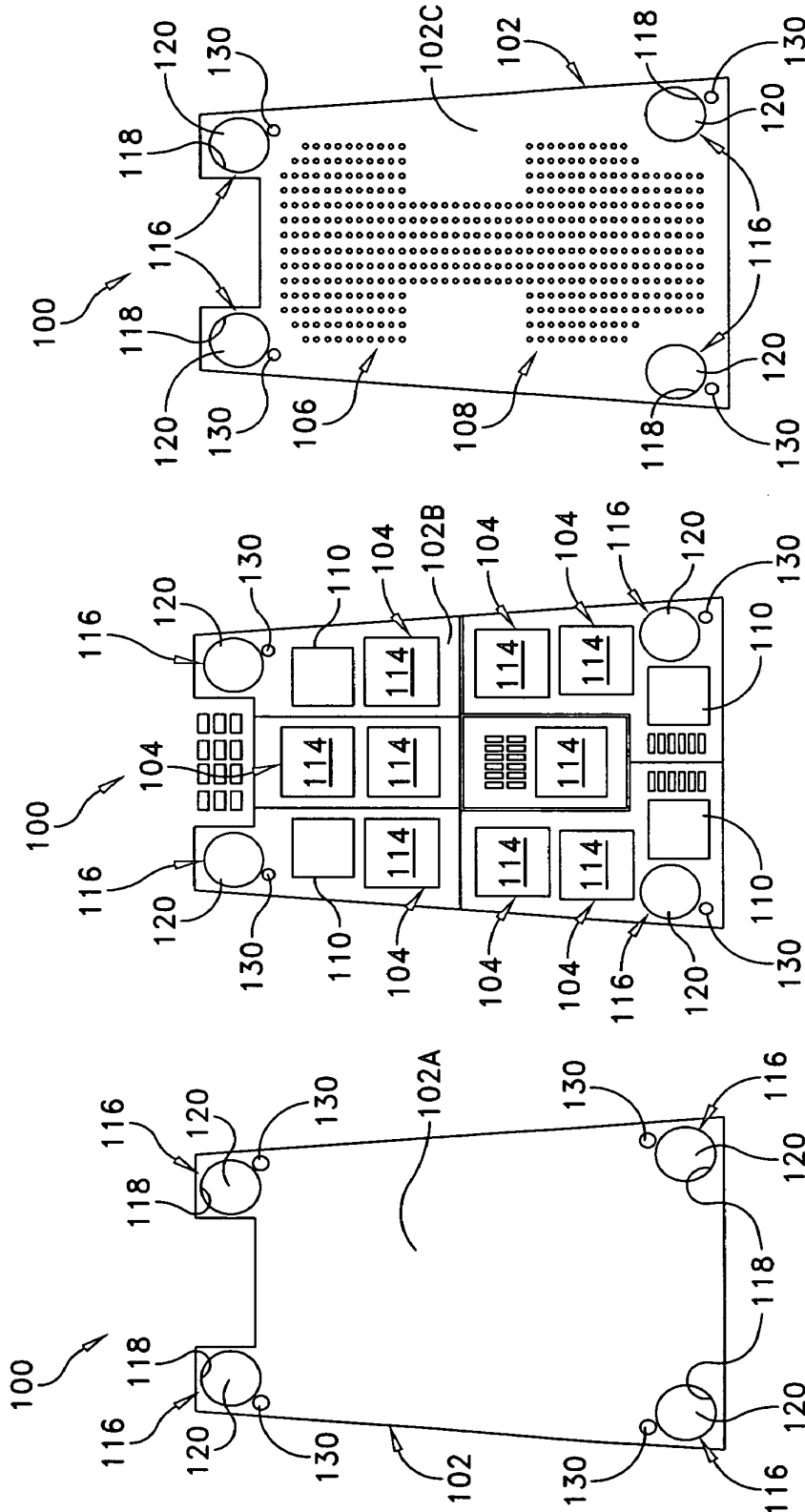


FIGURE 3

FIGURE 2

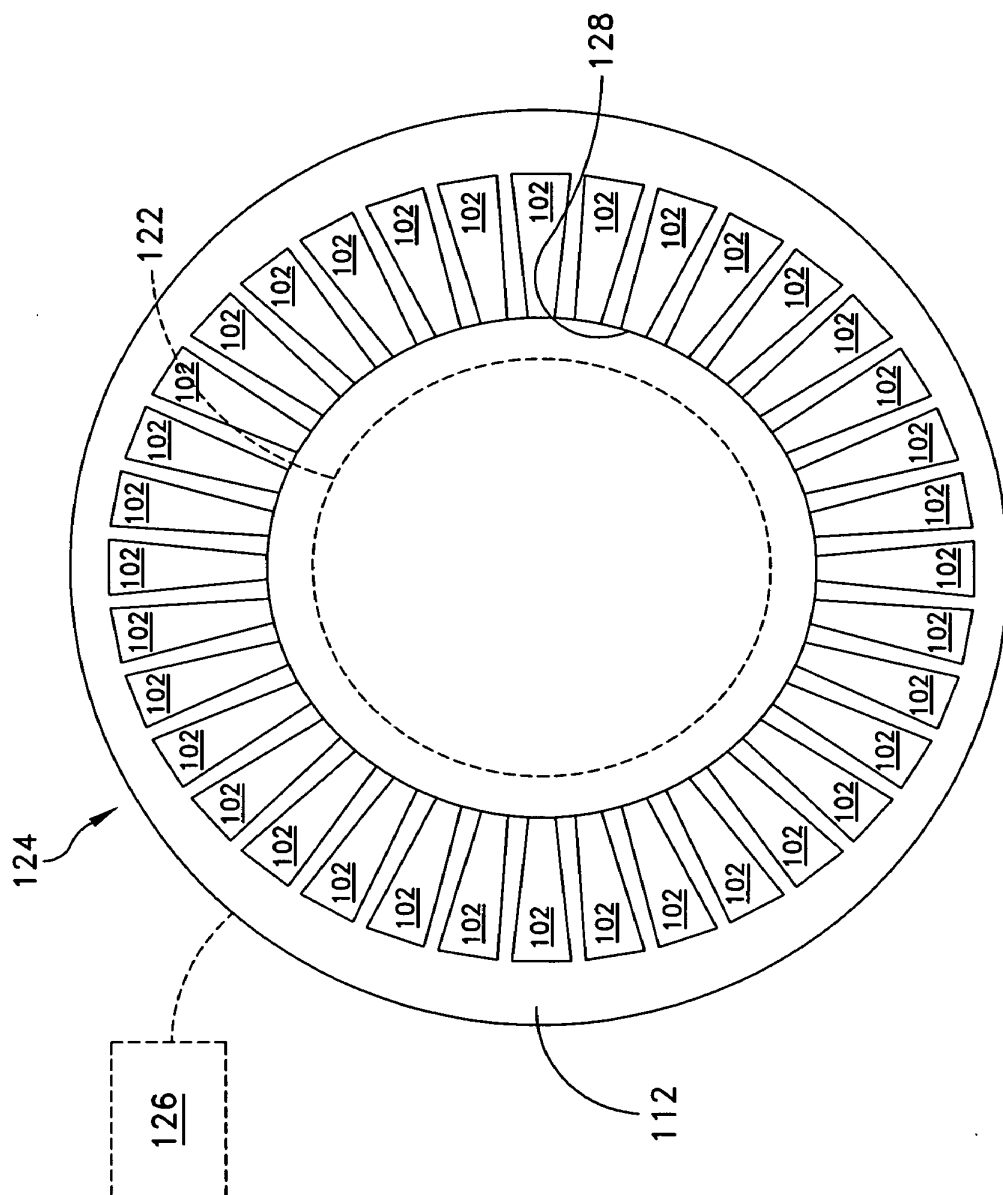
FIGURE 1

"APPARATUS, SYSTEMS AND METHODS FOR PROCESSING SIGNALS BETWEEN A TESTER AND A PLURALITY OF DEVICES UNDER TEST AT HIGH TEMPERATURES AND WITH SINGLE TOUCHDOWN OF A PROBE ARRAY"

Inventors: Romi Mayder, et al.

Docket No.: 10060220-1

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"APPARATUS, SYSTEMS AND METHODS FOR PROCESSING SIGNALS BETWEEN A TESTER AND A PLURALITY OF DEVICES UNDER TEST AT HIGH TEMPERATURES AND WITH SINGLE TOUCHDOWN OF A PROBE ARRAY"

Inventors: Romi Mayder, et al.

Docket No.: 10060220-1

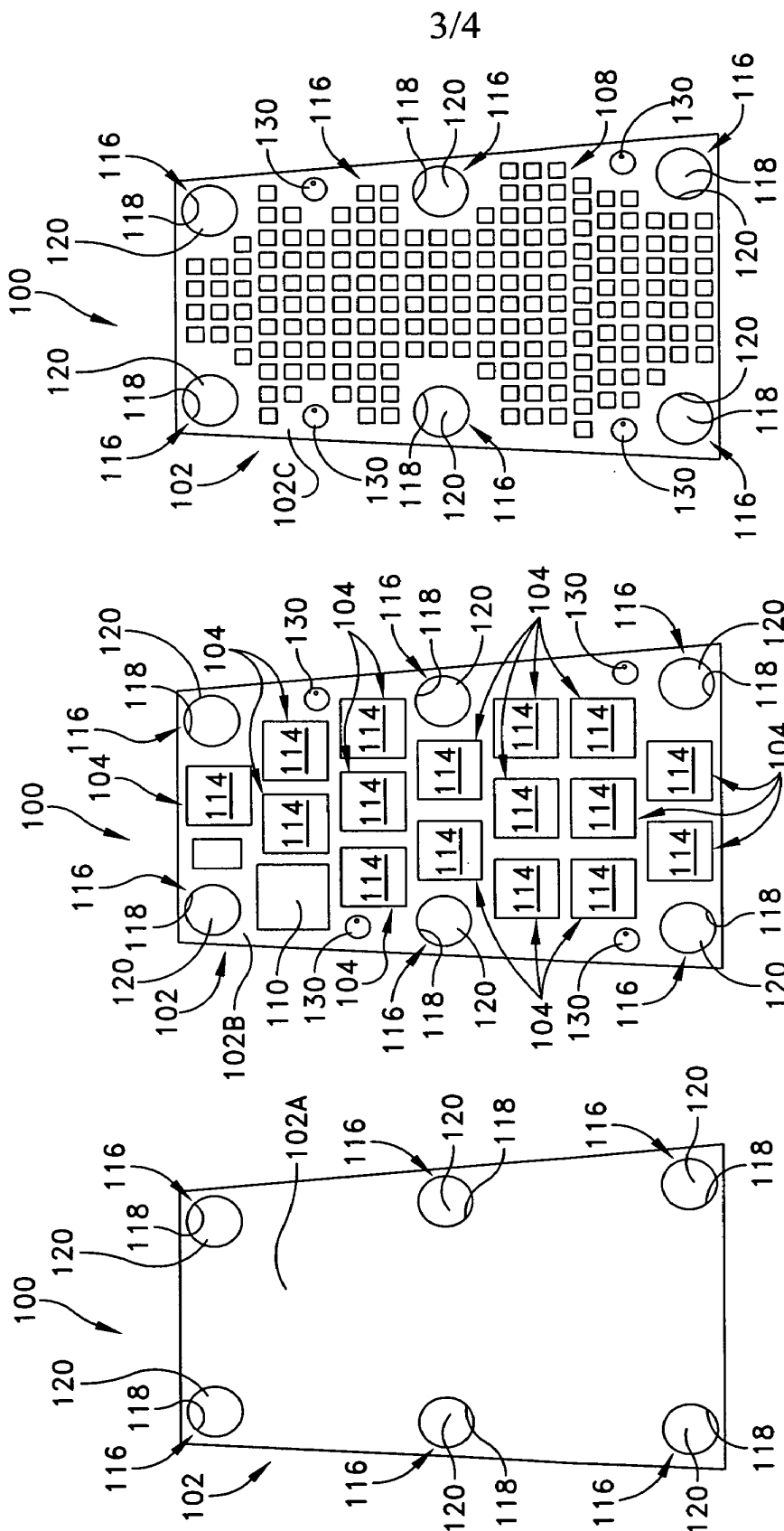


FIGURE 5

FIGURE 6

FIGURE 7

"APPARATUS, SYSTEMS AND METHODS FOR PROCESSING SIGNALS BETWEEN A TESTER AND A PLURALITY OF DEVICES UNDER TEST AT HIGH TEMPERATURES AND WITH SINGLE TOUCHDOWN OF A PROBE ARRAY"

Inventors: Romi Mayder, et al.

Docket No.: 10060220-1

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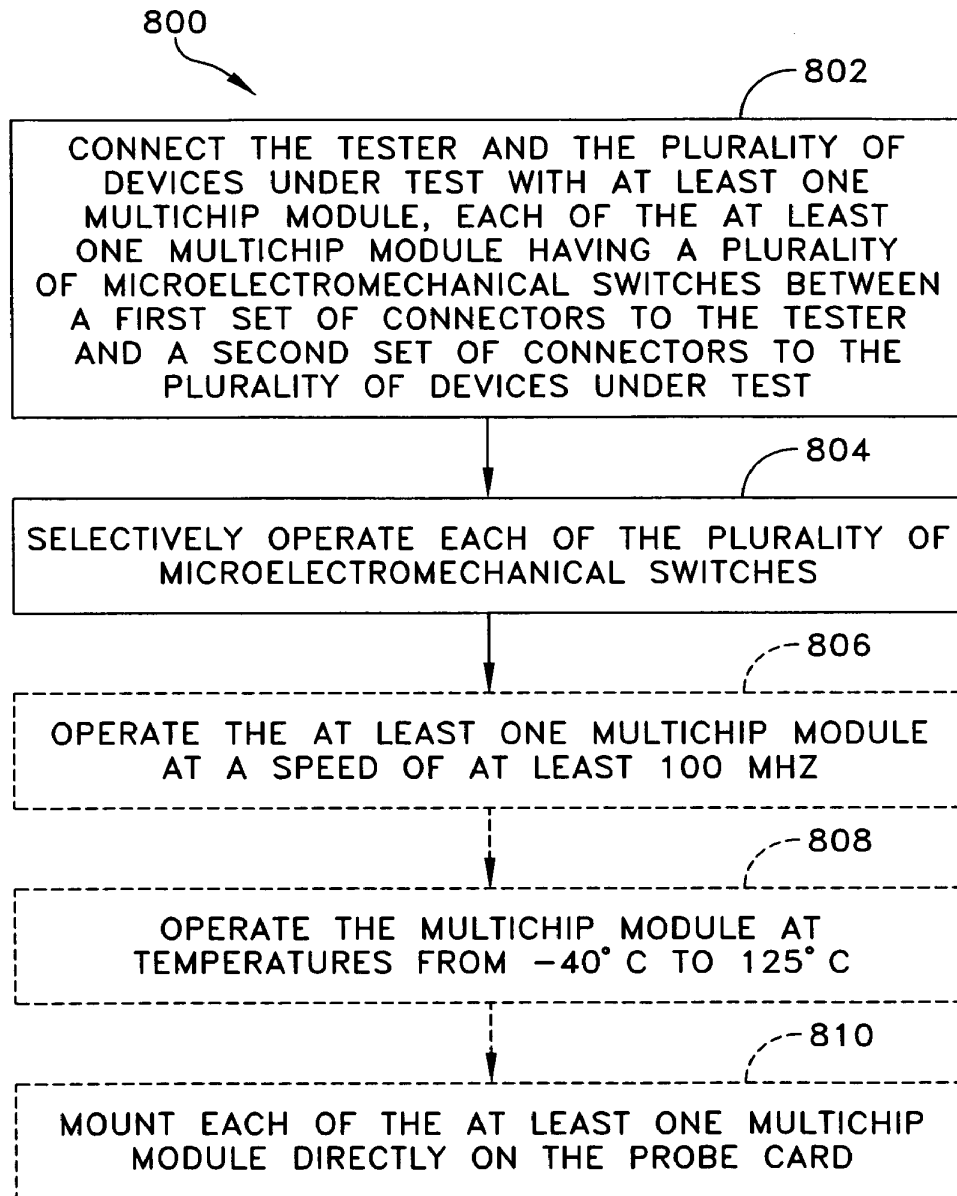


FIGURE 8

**DECLARATION AND POWER OF ATTORNEY
FOR PATENT APPLICATION****ATTORNEY DOCKET NO. 10060220-1**

As a below named inventor, I hereby declare that:

My residence/correspondence post office address and citizenship are as stated below next to my name:

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

APPARATUS, SYSTEMS AND METHODS FOR PROCESSING SIGNALS BETWEEN A TESTER AND A PLURALITY OF DEVICES UNDER TEST AT HIGH TEMPERATURES AND WITH SINGLE TOUCHDOWN OF A PROBE ARRAY

the specification of which is attached hereto unless the following box is checked:

☐ was filed on _____ as US Application Serial No. or PCT International Application
Number _____ and was amended on _____ (if applicable).

I hereby state that I have reviewed and understood the contents of the above-identified specification, including the claims, as amended by any amendment(s) referred to above. I acknowledge the duty to disclose all information which is material to patentability as defined in 37 CFR 1.56.

Foreign Application(s) and/or Claim of Foreign Priority

I hereby claim foreign priority benefits under Title 35, United States Code Section 119 of any foreign application(s) for patent or inventor(s) certificate listed below and have also identified below any foreign application for patent or inventor(s) certificate having a filing date before that of the application on which priority is claimed:

COUNTRY	APPLICATION NUMBER	DATE FILED	PRIORITY CLAIMED UNDER 35 U.S.C. 119
N/A			YES: <input type="checkbox"/> NO: <input type="checkbox"/>
			YES: <input type="checkbox"/> NO: <input type="checkbox"/>

Provisional Application

I hereby claim the benefit under Title 35, United States Code Section 119(e) of any United States provisional application(s) listed below:

APPLICATION SERIAL NUMBER	FILING DATE
N/A	

U. S. Priority Claim

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code Section 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, Section 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

APPLICATION SERIAL NUMBER	FILING DATE	STATUS (patented/pending/abandoned)
N/A		

POWER OF ATTORNEY:

As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith: PRACTITIONERS ASSOCIATED WITH CUSTOMER NUMBER 022878.

Send Correspondence to :**Direct Telephone Calls To:****Customer Number** 022878
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 OR **Gregory W. Osterloth**
 (303) 291-3204

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of Inventor: Romi Mayder**Residence:** San Jose, California**Correspondence Post Office Address:** P.O. Box 7599, Loveland, Colorado 80537-0599**Citizenship:** U.S.A.

Inventor's Signature

Date

Apr. 24, 2006

**DECLARATION AND POWER OF ATTORNEY
FOR PATENT APPLICATION (Continued)**

ATTORNEY DOCKET NO. 10060220-1

Full Name of # 2 Joint Inventor: Pam Stelmacher
Residence: Cupertino, California

Citizenship: U.S.A.

Correspondence Post Office Address: P.O. Box 7599, Loveland, Colorado 80537-0599

Pam Stelmacher
Inventor's Signature

4/24/06
Date

Full Name of # 3 Joint Inventor: Edmundo Dela Puente
Residence: Cupertino, California

Citizenship:

Correspondence Post Office Address: P.O. Box 7599, Loveland, Colorado 80537-0599

Edmundo Dela Puente
Inventor's Signature

4/24/06
Date

Full Name of # 4 Joint Inventor: John Andberg
Residence: Santa Cruz, California

Citizenship:

Correspondence Post Office Address: P.O. Box 7599, Loveland, Colorado 80537-0599

John Andberg
Inventor's Signature

4/24/06
Date

Full Name of # Joint Inventor:

Citizenship:

Residence:

Correspondence Post Office Address:

Inventor's Signature

Date

Full Name of # Joint Inventor:

Citizenship:

Residence:

Correspondence Post Office Address:

Inventor's Signature

Date

Full Name of # Joint Inventor:

Citizenship:

Residence:

Correspondence Post Office Address:

Inventor's Signature

Date

Full Name of # Joint Inventor:

Citizenship:

Residence:

Correspondence Post Office Address:

Inventor's Signature

Date

Full Name of # Joint Inventor:

Citizenship:

Residence:

Correspondence Post Office Address:

Inventor's Signature

Date

PATENT APPLICATION SERIAL NO. _____

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE
FEE RECORD SHEET

04/27/2006 HLE333 00000038 501078 11410699

01 FC:1011	300.00 DA
02 FC:1111	500.00 DA
03 FC:1311	200.00 DA
04 FC:1201	200.00 DA
05 FC:1202	150.00 DA

PTO-1556
(5/87)

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875 Effective December 8, 2004

Application or Docket Number

11410649

APPLICATION AS FILED - PART I

(Column 1)

(Column 2)

SMALL ENTITY

OR

OTHER THAN SMALL ENTITY

FOR	NUMBER FILED	NUMBER EXTRA
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A
SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A
EXAMINATION FEE (37 CFR 1.16(d), (e), or (f))	N/A	N/A
TOTAL CLAIMS (37 CFR 1.16(i))	23 minus 20 =	3
INDEPENDENT CLAIMS (37 CFR 1.16(h))	4 minus 3 =	1
APPLICATION SIZE FEE (37 CFR 1.16(e))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).	
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))		

RATE (\$)	FEE (\$)
N/A	150.00
N/A	\$250
N/A	\$100
X\$ 25 =	
X100 =	
+180=	
TOTAL	

RATE (\$)	FEE (\$)
N/A	300.00
N/A	\$500
N/A	\$200
X\$50 =	150
X200 =	200
+360=	
TOTAL	1850

* If the difference in column 1 is less than zero, enter "0" in column 2.

APPLICATION AS AMENDED - PART II

(Column 1)

(Column 2)

(Column 3)

SMALL ENTITY

OR

OTHER THAN SMALL ENTITY

AMENDMENT A	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total (37 CFR 1.16(i))	•	Minus **	=
Independent (37 CFR 1.16(h))	•	Minus ***	=
Application Size Fee (37 CFR 1.16(s))			
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))			

RATE (\$)	ADDITIONAL FEE (\$)
X\$ 25 =	
X100 =	
+180=	
TOTAL ADD'L FEE	

RATE (\$)	ADDITIONAL FEE (\$)
X\$50 =	
X200 =	
+360=	
TOTAL ADD'L FEE	

(Column 1)

(Column 2)

(Column 3)

AMENDMENT B	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total (37 CFR 1.16(i))	•	Minus **	=
Independent (37 CFR 1.16(h))	•	Minus ***	=
Application Size Fee (37 CFR 1.16(s))			
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))			

RATE (\$)	ADDITIONAL FEE (\$)
X\$ 25 =	
X100 =	
+180=	
TOTAL ADD'L FEE	

RATE (\$)	ADDITIONAL FEE (\$)
X\$50 =	
X200 =	
+360=	
TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.



UNITED STATES PATENT AND TRADEMARK OFFICE

COMMISSIONER FOR PATENTS
UNITED STATES PATENT AND TRADEMARK OFFICE
WASHINGTON, D.C. 20231
www.uspto.gov

APPLICATION NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NUMBER
11/410,699	04/24/2006	Romi Mayder	10060220-1

CONFIRMATION NO. 4586

NOTICE OF INFORMAL APPLICATION

This application is considered to be informal since it does not comply with the regulations for the reason(s) indicated below. The period within to correct the informalities noted below and avoid abandonment is set in the accompanying Office action.

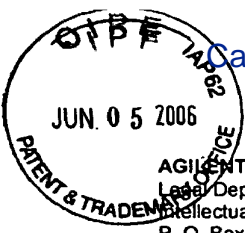
Items Required To Avoid Processing Delays:

The item(s) indicated below are also required and should be submitted with any reply to this notice to avoid further processing delays.

A new oath or declaration, identifying this application number is required. The oath or declaration does not comply with 37 CFR 1.63 in that it:

- does not identify the citizenship of each inventor.

OFFICE COPY



AGILENT TECHNOLOGIES, INC.
Legal Department, DL429
Intellectual Property Administration
P. O. Box 7599
Loveland, Colorado 80537-0599

ATTORNEY DOCKET NO. 10060220-1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Romi Mayder, et al.

Serial No.: 11/410,699

Examiner: Not Yet Assigned

Filing Date: April 24, 2006

Group Art Unit: Unknown

Title: APPARATUS, SYSTEMS AND METHODS FOR PROCESSING SIGNALS BETWEEN A TESTER AND A PLURALITY OF DEVICES UNDER TEST AT HIGH TEMPERATURES AND WITH SINGLE TOUCHDOWN OF A PROBE ARRAY

COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria VA 22313-1450

TRANSMITTAL LETTER FOR RESPONSE/AMENDMENT

Sir:

Transmitted herewith is/are the following in the above-identified application:

- ☐ Response/Amendment ☐ Petition to extend time to respond
☐ New fee as calculated below ☒ Submission of Supplemental Declaration and Power of Attorney
☒ No additional fee (Address envelope to "Mail Stop Amendments")
☐ Other: (Fee \$)

CLAIMS AS AMENDED BY OTHER THAN A SMALL ENTITY						
(1) FOR	(2) CLAIMS REMAINING AFTER AMENDMENT	(3) NUMBER EXTRA	(4) HIGHEST NUMBER PREVIOUSLY PAID FOR	(5) PRESENT EXTRA	(6) RATE	(7) ADDITIONAL FEES
TOTAL CLAIMS	23	MINUS	23	= 0	X 50	\$ 0
INDEP. CLAIMS	4	MINUS	4	= 0	X 200	\$ 0
<input type="checkbox"/> FIRST PRESENTATION OF A MULTIPLE DEPENDENT CLAIM					+ 360	\$ 0
EXTENSION FEE	1 ST MONTH 120.00 <input type="checkbox"/>	2 ND MONTH 450.00 <input type="checkbox"/>	3 RD MONTH 1020.00 <input type="checkbox"/>	4 TH MONTH 1590.00 <input type="checkbox"/>		\$ 0
OTHER FEES						\$ 0
TOTAL ADDITIONAL FEE FOR THIS AMENDMENT						\$ 0

Charge \$ 0 to Deposit Account 50-1078. At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account 50-1078 pursuant to 37 CFR 1.25. Additionally please charge any fees to Deposit Account 50-1078 under 37 CFR 1.16, 1.17, 1.19, 1.20 and 1.21. A duplicate copy of this transmittal letter is enclosed.

Respectfully submitted,

Romi Mayder, et al.

By James A. Sheridan
James A. Sheridan
Attorney/Agent for Applicant(s) 6/1/06

I hereby certify that this correspondence is being Deposited with the United States Postal Service as First class mail in an envelope addressed to: Commissioner for Patents, PO Box 1450, Alexandria, VA 22313-1450.

Date of Deposit: June 1, 2006

Typed Name: Chasity C. Rossum

Signature: Chasity C. Rossum

Reg. No. 43,114

Date: June 1, 2006

Telephone No. (303) 291-3200

AGILENT TECHNOLOGIES, INC.
Legal department, DL429
Intellectual Property Administration
P.O. Box 7599
Loveland, Colorado 80537-0599

ATTORNEY DOCKET NO. 10060220-1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Romi Mayder, et al.

Serial No.: 11/410,699

Examiner: Not Yet Assigned

Filing Date: April 24, 2006

Group Art Unit: Unknown

Title: APPARATUS, SYSTEMS AND METHODS FOR PROCESSING SIGNALS
BETWEEN A TESTER AND A PLURALITY OF DEVICES UNDER TEST AT
HIGH TEMPERATURES AND WITH SINGLE TOUCHDOWN OF A PROBE
ARRAY

COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, VA 22313-1450

**SUBMISSION OF SUPPLEMENTAL
DECLARATION AND POWER OF ATTORNEY**

Sir:

Upon review of the Declaration and Power of Attorney originally filed on April 24, 2006, submitted herewith is a supplemental Declaration and Power of Attorney.

Applicants note that the Declaration and Power of Attorney originally filed on April 24, 2006 does not identify the citizenship of two of the inventors, specifically Edmundo Dela Puente and John Andberg. Applicants respectfully request entry of the supplemental Declaration and Power of Attorney.

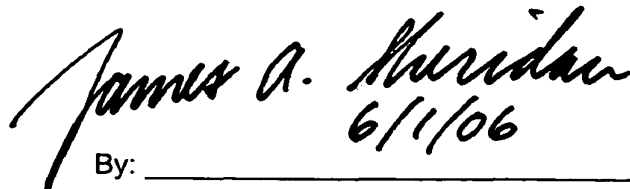
Respectfully submitted,

Romi Mayder, et al.

I hereby certify that this correspondence is being deposited in the United States Postal Service as First Class mail address to the United States Patent and Trademark Office, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Date of Deposit: June 1, 2006

By: 
Chasity C. Rossum


By: _____

James A. Sheridan

Registration No. 43,114

Date: June 1, 2006

Telephone No.: (303) 291-3200

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Page 1 of 2

Rev 09/05 (DacPw)

Full Name of Inventor: Romi Mayder
 Residence: San Jose, California
 Correspondence Post Office Address: P.O. Box 7599, Loveland, Colorado 80537-0599
 Inventor's Signature: *[Signature]*
 Date: *May 09, 2006*
 Citizenship: U.S.A.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Send Correspondence to: **AGILENT TECHNOLOGIES, INC.**
 Legal Department, DL 429
 Intellectual Property Administration
 P.O. Box 7599
 Loveland, Colorado 80537-0599
 Customer Number: **022878**
 Cynthia S. Mitchell (970) 679-3136
 OR
 Gregory W. Osterloth (303) 291-3204
 Direct Telephone Calls To:

As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith: PRACTITIONERS ASSOCIATED WITH CUSTOMER NUMBER 022878.

POWER OF ATTORNEY:	APPLICATION SERIAL NUMBER	FILING DATE	STATUS (patented/pending/abandoned)
	N/A		

U.S. Priority Claim

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code Section 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, Section 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

APPLICATION SERIAL NUMBER	FILING DATE
N/A	

I hereby claim the benefit under Title 35, United States Code Section 119(e) of any United States provisional application(s) listed below:

PROVISIONAL APPLICATION	APPLICATION NUMBER	DATE FILED	PRIORITY CLAIMED UNDER 35 U.S.C. 119
N/A			YES: <input type="checkbox"/> NO: <input type="checkbox"/>

Foreign Application(s) and/or Claim of Foreign Priority

I hereby claim foreign priority benefits under Title 35, United States Code Section 119 of any foreign application(s) for patent or inventor(s) certificate listed below and have also identified below any foreign application for patent or inventor(s) certificate having a filing date before that of the application on which priority is claimed:

I hereby state that I have reviewed and understood the contents of the above-identified specification, including the claims, as amended by any amendment(s) referred to above. I acknowledge the duty to disclose all information which is material to patentability as defined in 37 CFR 1.56.

Number 11/410699 and was amended on _____ (if applicable).

☒ was filed on April 24, 2008 as US Application Serial No. or PCT International Application

the specification of which is attached hereto unless the following box is checked:

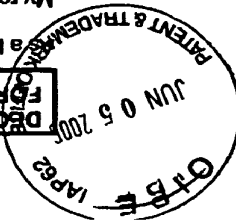
APPARATUS, SYSTEMS AND METHODS FOR PROCESSING SIGNALS BETWEEN A TESTER AND A PLURALITY OF DEVICES UNDER TEST AT HIGH TEMPERATURES AND WITH SINGLE TOUCHDOWN OF A PROBE ARRAY

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

My residence/correspondence post office address and citizenship are as stated below next to my name:

a below named inventor, I hereby declare that:

DECLARATION AND POWER OF ATTORNEY
 FOR PATENT APPLICATION
 ATTORNEY DOCKET NO. 10060220-1



**DECLARATION AND POWER OF ATTORNEY
FOR PATENT APPLICATION (Continued)**

ATTORNEY DOCKET NO. 10060220-1

Full Name of # 2 Joint Inventor: Pam Stelmacher
Residence: Cupertino, California
Correspondence Post Office Address: P.O. Box 7599, Loveland, Colorado 80537-0599

Citizenship: U.S.A.

Pam Stelmacher
Inventor's Signature

May 9, 2006
Date

Full Name of # 3 Joint Inventor: Edmundo Dela Puente
Residence: Cupertino, California
Correspondence Post Office Address: P.O. Box 7599, Loveland, Colorado 80537-0599

Citizenship: U.S.A.

Edmundo Dela Puente
Inventor's Signature

May 9, 2006
Date

Full Name of # 4 Joint Inventor: John Andberg
Residence: Santa Cruz, California
Correspondence Post Office Address: P.O. Box 7599, Loveland, Colorado 80537-0599

Citizenship: U.S.A.

John Andberg
Inventor's Signature

May 9, 06
Date

Full Name of # Joint Inventor:
Residence:
Correspondence Post Office Address:

Citizenship:

Inventor's Signature

Date

Full Name of # Joint Inventor:
Residence:
Correspondence Post Office Address:

Citizenship:

Inventor's Signature

Date

Full Name of # Joint Inventor:
Residence:
Correspondence Post Office Address:

Citizenship:

Inventor's Signature

Date

Full Name of # Joint Inventor:
Residence:
Correspondence Post Office Address:

Citizenship:

Inventor's Signature

Date

Full Name of # Joint Inventor:
Residence:
Correspondence Post Office Address:

Citizenship:

Inventor's Signature

Date

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EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	40	tester and (switch with transistor or transistor adj switch) and controller and module and "324"/\$.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2007/03/27 10:59
L2	137	tester and (switch with transistor or transistor adj switch) and controller and "324"/\$.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2007/03/27 11:51
L3	78593	mem and switch	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2007/03/27 11:51
L4	110	3 and tester and relay and controller	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2007/03/27 11:58
L5	43	mem same switch same interposer not cell	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2007/03/27 11:59
L6	5	324/754.ccls. and mem same switch	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2007/03/27 12:00
L7	0	verlgy.as.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2007/03/27 12:13
L8	12036	agilent.as.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2007/03/27 12:13

EAST Search History

L9	143	8 and mem	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2007/03/27 12:39
L10	2	"6339338".pn.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2007/03/27 12:48
L11	2	"6657455".pn.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2007/03/27 12:48
L12	0	eldridge.in. and electromechanical adj switch	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2007/03/27 13:22
L13	0	eldridge.in. and electro adj mechanical adj switch	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2007/03/27 13:22
L14	0	eldridge.in. and electrical with mechanical adj switch	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2007/03/27 13:22
L15	0	324/754.ccls. and electrical with mechanical adj switch	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2007/03/27 13:23
L16	69	"324"/\$.ccls. and electrical with mechanical adj switch	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2007/03/27 13:36

EAST Search History

L17	0	electrical with mechanical adj switch same probe adj card	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2007/03/27 13:36
L18	4	electrical with mechanical adj switch and probe adj card	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2007/03/27 14:10
L19	2	"6657455".pn.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2007/03/27 14:26
L20	83	324/765.ccls. and probe adj card and temperature and frequency	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2007/03/27 14:48
L21	19	324/765.ccls. and probe adj card and temperature same frequency	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2007/03/27 14:54
L22	42	324/765.ccls. and probe adj card and temperature same "100"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2007/03/27 14:55
L23	10	324/765.ccls. and probe adj card and temperature same "125"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2007/03/27 15:37
L24	12	"324"/\$.ccls. and burn adj in and probe adj card and "125" same degrees	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2007/03/27 15:42

EAST Search History

L25	2	"6812718".pn.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2007/03/27 15:41
L26	2	"7009412".pn.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2007/03/27 15:41
L27	4	burn adj in same "125" same degrees	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2007/03/27 15:43
L28	0	burn adj in same degrees	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2007/03/27 15:43
L29	9	burn adj in same degrees	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2007/03/27 15:47
L30	0	in same order same test same sensitivity same timing wame write same operations same cpu	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2007/03/27 15:48
L31	4	in same order same test same sensitivity same timing same write same operations same cpu	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2007/03/27 15:48
L32	7	4 and testing adj scenario	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2007/03/27 15:48

EAST Search History

L33	4	31 and testing adj scenario	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2007/03/27 16:07
L34	313	burn with in same temperature same degrees and @py<"2004"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2007/03/27 16:08
L35	44	"324"/\$.ccls. and burn with in same temperature same degrees and @py<"2004"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2007/03/27 16:08



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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Alexandria, Virginia 22313-1450
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/410,699	04/24/2006	Romi Mayder	10060220-1	4586

22878 7590 04/03/2007

AGILENT TECHNOLOGIES INC.
INTELLECTUAL PROPERTY ADMINISTRATION, LEGAL DEPT.
MS BLDG. E P.O. BOX 7599
LOVELAND, CO 80537

EXAMINER

ISLA RODAS, RICHARD

ART UNIT	PAPER NUMBER
----------	--------------

2829

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/03/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary

Application No.

11/410,699

Applicant(s)

MAYDER ET AL.

Examiner

Richard Isla-Rodas

Art Unit

2829

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 24 April 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-23 is/are pending in the application.
- 4a) Of the above claim(s) 1-18 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 19-23 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 24 April 2006 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____.

- 4) ☒ Interview Summary (PTO-413)
Paper No(s)/Mail Date. 3/26/07.
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____.

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DETAILED ACTION

Election/Restrictions

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:
 - I. Claims 1-18, drawn to an Apparatus and system for processing signals, classified in class 324, subclass 754.
 - II. Claims 19-23, drawn to a method of processing signals at speeds of 100 Mhz, classified in class 324, subclass 765.
2. The inventions are distinct, each from the other because of the following reasons:

Inventions II and I are related as process and apparatus for its practice. The inventions are distinct if it can be shown that either: (1) the process as claimed can be practiced by another and materially different apparatus or by hand, or (2) the apparatus as claimed can be used to practice another and materially different process. (MPEP § 806.05(e)). In this case the apparatus of Group I can be used to calibrate a tester by connecting a tester to a calibration chip, wherein the switches are used to block/allow the passing of information from the chips to the tester.
2. Because these inventions are independent or distinct for the reasons given above and there would be a serious burden on the examiner if restriction is not required because the inventions have acquired a separate status in the art in view of their different classification, restriction for examination purposes as indicated is proper.
3. Because these inventions are independent or distinct for the reasons given above and there would be a serious burden on the examiner if restriction is not required

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because the inventions require a different field of search (see MPEP § 808.02), restriction for examination purposes as indicated is proper.

4. Because these inventions are independent or distinct for the reasons given above and there would be a serious burden on the examiner if restriction is not required because the inventions have acquired a separate status in the art due to their recognized divergent subject matter, restriction for examination purposes as indicated is proper.

5. If Group I is elected, **a further election of species is required** as follows:

- Species of Figures 1, 2 and 3
- Species of Figures 5, 6 and 7

6. The species are independent or distinct because they each disclose patentably different embodiments of the same inventive idea.

Applicant is required under 35 U.S.C. 121 to elect a single disclosed species for prosecution on the merits to which the claims shall be restricted if no generic claim is finally held to be allowable. Currently, no claim appears generic.

Applicant is advised that a reply to this requirement must include an identification of the species that is elected consonant with this requirement, and a listing of all claims readable thereon, including any claims subsequently added. An argument that a claim is allowable or that all claims are generic is considered nonresponsive unless accompanied by an election.

Upon the allowance of a generic claim, applicant will be entitled to consideration of claims to additional species which depend from or otherwise require all the limitations

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of an allowable generic claim as provided by 37 CFR 1.141. If claims are added after the election, applicant must indicate which are readable upon the elected species.

MPEP § 809.02(a).

7. During a telephone conversation with Cynthia Mitchell on March 3, 2007 a provisional election was made without traverse to prosecute the invention of Group II, claims 19-23. Affirmation of this election must be made by applicant in replying to this Office action. Claims 1-18 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Claim Rejections - 35 USC § 101

8. 35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

9. Claims 19-23 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Claims 19-23 recite a method for processing signals. As such, the claims are directed to an abstract idea (judicial exception). In order to be eligible for patenting, they need to provide a practical application by physical transformation or a useful, concrete, and tangible result. These claims are nonstatutory because they do not have physical transformation or a tangible result. That is, the steps of "selectively operating a set of switches" do not provide a physical transformation of a device nor a tangible result.

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Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

11. Claims 19 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over the US Patent to Eldridge et al. 6,657,455 (Eldridge hereinafter).

In terms of claim 19, Eldridge teaches in Figure 9, a method comprising the steps of connecting a tester (58) and a plurality of devices under test (34) with a multichip (a unit that is capable of connecting to a plurality of chips) module (52), having a plurality of micro electrical switches (Sw2) between a set of connectors to the tester (connectors transmitting signals SYSCLK as well as START) and a second set of connectors to the plurality of devices under test (probes 37 connecting to each switch to its respective DUT as explained in lines 52-54, column 7) and selectively operating each of the plurality of micro electrical switches. As explained in lines 14-16 column 6, the tester 30 controls the states of switches Sw2. That is the tester selectively operate whether they are in the "on" or off" position. Eldridge substantially teaches all of the claimed elements discussed above, except for explicitly stating that switches Sw2 are "electro-mechanical." Although Eldridge clearly shows the switches to be electrical, there is no "explicit" mention that they are also mechanical. However, it has been held that to be entitled to weight in method claims, the recited-structure limitations therein must affect

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the method in a manipulative sense, and not to amount to the mere claiming of a use of a particular structure. Ex parte Pfeiffer, 1962 C.D. 408 (1961). Therefore, since the electrical switch performs the exact same recited method step (that of connecting the tester to the devices under test), it is its functional equivalent. The choice of using "electro-mechanical" switches over "electrical" switches does not differentiate the claimed method from the method taught by the prior art, since the "electrical" switches perform the method step in a functionally equivalent fashion.

As to claim 22, Eldridge shows the multichip module (52) is mounted directly on a probe card (50).

12. Claims 20, 21 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Eldridge in view of the US Patent to McCord 6,681,869 (McCord hereinafter) in view of the US Patent to Akram (6,640,323).

As to claims 20, 21 and 23, Eldridge substantially teaches all of the claimed steps as discussed above, except for the step of operating the multichip module at a speed (frequency) of at least 100 MHz. McCord shows that it's well known in the art that to operate a tester (and consequently the module connecting it to the device under test) at and above the rated clock frequency of the device under test (see lines 29-38 in column 10). For instance, when testing a device which working frequency is 533 MHz, is customary to process the signals at frequencies up to 584MHz. It would have been obvious to one of ordinary skill in the art, to operate the multichip module at 100MHz or more when testing devices whose frequency of operation is below such frequency, as

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taught by McCord, in order to replicate the working conditions of said devices.

Furthermore, Eldridge in view of McCord is silent as to the preferred temperature of operation of the device. Akram teaches a procedure known as static method of burn-in that consist of applying test signals on devices under test at temperatures of 125 degrees Celsius. Such method comprises the step of applying operating voltages on the devices under test that are much higher than their normal operating voltage, thereby increasing the temperature of the devices under test and removing those devices that fail to withstand the temperature and/or voltage (infant mortality of dies), as explained in lines 21-32 in column 2. It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to apply higher than normal operating voltages on the devices under test (by operating the multichip module to send higher than normal test signals to the devices under test) thereby increasing the temperature of operation to up to 125 degrees, as taught by Akram, in order to detect early failure of the devices under test (infant mortality of dies) as suggested by Akram in line 10 of column 2.

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. US Patents to Ellingboe et al. (6,490,536), Sunter (6,703,820) and US Patent Application by Akram (2003/0057984).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Richard Isla-Rodas whose telephone number is (571)

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272-5056. The examiner can normally be reached on Monday through Friday 8 am to 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ha Nguyen can be reached on (571) 272-1678. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Richard Isla-Rodas
March 27, 2007



HA TRAN NGUYEN
SUPERVISORY PATENT EXAMINER

Interview Summary	Application No.		Applicant(s)	
	11/410,699		MAYDER ET AL.	
	Examiner		Art Unit	
	Richard Isla-Rodas		2829	

All participants (applicant, applicant's representative, PTO personnel):

(1) Richard Isla-Rodas. (3) _____

(2) Cynthia Mitchell. (4) _____

Date of Interview: 26 March 2007.

Type: a) ☒ Telephonic b) ☐ Video Conference
c) ☐ Personal [copy given to: 1) ☐ applicant 2) ☐ applicant's representative]

Exhibit shown or demonstration conducted: d) ☐ Yes e) ☐ No.
If Yes, brief description: _____

Claim(s) discussed: 1-23.

Identification of prior art discussed: _____

Agreement with respect to the claims f) ☒ was reached. g) ☐ was not reached. h) ☐ N/A.

Substance of Interview including description of the general nature of what was agreed to if an agreement was reached, or any other comments: Ms. Cynthia Mitchell was contacted to request an oral election of Groups. Ms. Mitchell elected Group II drawn to claims 19-23 without traverse.

(A fuller description, if necessary, and a copy of the amendments which the examiner agreed would render the claims allowable, if available, must be attached. Also, where no copy of the amendments that would render the claims allowable is available, a summary thereof must be attached.)

THE FORMAL WRITTEN REPLY TO THE LAST OFFICE ACTION MUST INCLUDE THE SUBSTANCE OF THE INTERVIEW. (See MPEP Section 713.04). If a reply to the last Office action has already been filed, APPLICANT IS GIVEN A NON-EXTENDABLE PERIOD OF THE LONGER OF ONE MONTH OR THIRTY DAYS FROM THIS INTERVIEW DATE, OR THE MAILING DATE OF THIS INTERVIEW SUMMARY FORM, WHICHEVER IS LATER, TO FILE A STATEMENT OF THE SUBSTANCE OF THE INTERVIEW. See Summary of Record of Interview requirements on reverse side or on attached sheet.

Examiner Note: You must sign this form unless it is an Attachment to a signed Office action.

Examiner's signature, if required

Summary of Record of Interview Requirements

Manual of Patent Examining Procedure (MPEP), Section 713.04, Substance of Interview Must be Made of Record

A complete written statement as to the substance of any face-to-face, video conference, or telephone interview with regard to an application must be made of record in the application whether or not an agreement with the examiner was reached at the interview.

Title 37 Code of Federal Regulations (CFR) § 1.133 Interviews

Paragraph (b)

In every instance where reconsideration is requested in view of an interview with an examiner, a complete written statement of the reasons presented at the interview as warranting favorable action must be filed by the applicant. An interview does not remove the necessity for reply to Office action as specified in §§ 1.111, 1.135. (35 U.S.C. 132)

37 CFR §1.2 Business to be transacted in writing.

All business with the Patent or Trademark Office should be transacted in writing. The personal attendance of applicants or their attorneys or agents at the Patent and Trademark Office is unnecessary. The action of the Patent and Trademark Office will be based exclusively on the written record in the Office. No attention will be paid to any alleged oral promise, stipulation, or understanding in relation to which there is disagreement or doubt.

The action of the Patent and Trademark Office cannot be based exclusively on the written record in the Office if that record is itself incomplete through the failure to record the substance of interviews.

It is the responsibility of the applicant or the attorney or agent to make the substance of an interview of record in the application file, unless the examiner indicates he or she will do so. It is the examiner's responsibility to see that such a record is made and to correct material inaccuracies which bear directly on the question of patentability.

Examiners must complete an Interview Summary Form for each interview held where a matter of substance has been discussed during the interview by checking the appropriate boxes and filling in the blanks. Discussions regarding only procedural matters, directed solely to restriction requirements for which interview recordation is otherwise provided for in Section 812.01 of the Manual of Patent Examining Procedure, or pointing out typographical errors or unreadable script in Office actions or the like, are excluded from the interview recordation procedures below. Where the substance of an interview is completely recorded in an Examiners Amendment, no separate Interview Summary Record is required.

The Interview Summary Form shall be given an appropriate Paper No., placed in the right hand portion of the file, and listed on the "Contents" section of the file wrapper. In a personal interview, a duplicate of the Form is given to the applicant (or attorney or agent) at the conclusion of the interview. In the case of a telephone or video-conference interview, the copy is mailed to the applicant's correspondence address either with or prior to the next official communication. If additional correspondence from the examiner is not likely before an allowance or if other circumstances dictate, the Form should be mailed promptly after the interview rather than with the next official communication.

The Form provides for recordation of the following information:

- Application Number (Series Code and Serial Number)
- Name of applicant
- Name of examiner
- Date of interview
- Type of interview (telephonic, video-conference, or personal)
- Name of participant(s) (applicant, attorney or agent, examiner, other PTO personnel, etc.)
- An indication whether or not an exhibit was shown or a demonstration conducted
- An identification of the specific prior art discussed
- An indication whether an agreement was reached and if so, a description of the general nature of the agreement (may be by attachment of a copy of amendments or claims agreed as being allowable). Note: Agreement as to allowability is tentative and does not restrict further action by the examiner to the contrary.
- The signature of the examiner who conducted the interview (if Form is not an attachment to a signed Office action)

It is desirable that the examiner orally remind the applicant of his or her obligation to record the substance of the interview of each case. It should be noted, however, that the Interview Summary Form will not normally be considered a complete and proper recordation of the interview unless it includes, or is supplemented by the applicant or the examiner to include, all of the applicable items required below concerning the substance of the interview.

A complete and proper recordation of the substance of any interview should include at least the following applicable items:

- 1) A brief description of the nature of any exhibit shown or any demonstration conducted,
- 2) an identification of the claims discussed,
- 3) an identification of the specific prior art discussed,
- 4) an identification of the principal proposed amendments of a substantive nature discussed, unless these are already described on the Interview Summary Form completed by the Examiner,
- 5) a brief identification of the general thrust of the principal arguments presented to the examiner,
(The identification of arguments need not be lengthy or elaborate. A verbatim or highly detailed description of the arguments is not required. The identification of the arguments is sufficient if the general nature or thrust of the principal arguments made to the examiner can be understood in the context of the application file. Of course, the applicant may desire to emphasize and fully describe those arguments which he or she feels were or might be persuasive to the examiner.)
- 6) a general indication of any other pertinent matters discussed, and
- 7) if appropriate, the general results or outcome of the interview unless already described in the Interview Summary Form completed by the examiner.

Examiners are expected to carefully review the applicant's record of the substance of an interview. If the record is not complete and accurate, the examiner will give the applicant an extendable one month time period to correct the record.

Examiner to Check for Accuracy

If the claims are allowable for other reasons of record, the examiner should send a letter setting forth the examiner's version of the statement attributed to him or her. If the record is complete and accurate, the examiner should place the indication, "Interview Record OK" on the paper recording the substance of the interview along with the date and the examiner's initials.

Notice of References Cited	Application/Control No. 11/410,699	Applicant(s)/Patent Under Reexamination MAYDER ET AL.	
	Examiner Richard Isla-Rodas	Art Unit 2829	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-6,657,455	12-2003	Eldridge et al.	324/765
*	B	US-6,640,323	10-2003	Akram, Salman	714/724
*	C	US-6,801,869	10-2004	McCord, Don	702/117
*	D	US-6,490,536	12-2002	Ellingboe et al.	702/115
*	E	US-6,703,820	03-2004	Sunter, Stephen K.	324/76.15
*	F	US-2003/0057984	03-2003	Akram, Salman	324/755
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Search Notes



Application/Control No.

11/410,699

Examiner

Richard Isla-Rodas

Applicant(s)/Patent under Reexamination

MAYDER ET AL.

Art Unit

2829

SEARCHED

[illegible]

INTERFERENCE SEARCHED

Class	Subclass	Date	Examiner

SEARCH NOTES (INCLUDING SEARCH STRATEGY)

[illegible]



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	PATENT NUMBER	GROUP ART UNIT	FILE WRAPPER LOCATION
11/410,699		2829	28M1

Correspondence Address / Fee Address Change

The following fields have been set to Customer Number 63448 on 06/27/2007

- Correspondence Address
- Maintenance Fee Address

The address of record for Customer Number 63448 is:

VERIGY
4700 INNOVATION WAY, BLDG D1
FORT COLLINS, CO 80528

VERIGY
4700 Innovation Drive, Bldg. D1
Fort Collins, Colorado 80528

ATTORNEY DOCKET NO. 10060220-1

Ifw

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Romi Mayder, et al.

Serial No.: 11/410,699

Examiner: Richard Isla Rodas

Filing Date: April 24, 2006

Group Art Unit: 2829

Title: APPARATUS, SYSTEMS AND METHODS FOR PROCESSING SIGNALS BETWEEN A TESTER AND
A PLURALITY OF DEVICES UNDER TEST AT HIGH TEMPERATURES AND WITH SINGLE
TOUCHDOWN OF A PROBE ARRAY

COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria VA 22313-1450

TRANSMITTAL LETTER FOR RESPONSE/AMENDMENT

Sir:

Transmitted herewith is/are the following in the above-identified application:

- ☒ Response/Amendment ☐ Petition to extend time to respond
☐ New fee as calculated below ☐ Supplemental Declaration
☒ No additional fee (Address envelope to "Mail Stop Amendments")
☐ Other: (Fee \$ _____)

CLAIMS AS AMENDED BY OTHER THAN A SMALL ENTITY						
(1) FOR	(2) CLAIMS REMAINING AFTER AMENDMENT	(3) NUMBER EXTRA	(4) HIGHEST NUMBER PREVIOUSLY PAID FOR	(5) PRESENT EXTRA	(6) RATE	(7) ADDITIONAL FEES
TOTAL CLAIMS	23	MINUS	23	= 0	X 50	\$ 0
INDEP. CLAIMS	4	MINUS	4	= 0	X 200	\$ 0
<input type="checkbox"/> FIRST PRESENTATION OF A MULTIPLE DEPENDENT CLAIM					+ 360	\$ 0
EXTENSION FEE	1 ST MONTH 120.00 <input type="checkbox"/>	2 ND MONTH 450.00 <input type="checkbox"/>	3 RD MONTH 1020.00 <input type="checkbox"/>	4 TH MONTH 1590.00 <input type="checkbox"/>	\$ 0	
OTHER FEES						\$ 0
TOTAL ADDITIONAL FEE FOR THIS AMENDMENT						\$ 0

Charge \$ 0 to Deposit Account 08-2623. At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account 08-2623 pursuant to 37 CFR 1.2 5. Additionally please charge any fees to Deposit Account 08-2623 under 37 CFR 1.16, 1.17, 1.19, 1.20 and 1.21. A duplicate copy of this transmittal letter is enclosed.

Respectfully submitted,

Romi Mayder, et al.

I hereby certify that this correspondence is being Deposited
with the United States Postal Service as First class mail in an
envelope addressed to: Commissioner for Patents,
PO Box 1450, Alexandria, VA 22313-1450.

Date of Deposit: July 3, 2007

Typed Name: James A. Sheridan

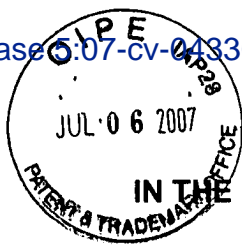
Signature: *James A. Sheridan*
7/3/07

By *James A. Sheridan*
James A. Sheridan
Attorney/Agent for Applicant(s) 7/3/07

Reg. No. 43,114

Date: July 3, 2007

Telephone No. (303) 295-8000



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appl. No. : 11/410,699 Confirmation No. 4586
Applicant : Romi Mayder, et al.
Filed : 04/24/2006
TC/A.U. : 2829
Examiner : Isla Rodas, Richard
Docket No. : 10060220-1

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT

Sir:

In response to the Office Action of April 3, 2007, please amend the above-identified application as follows:

Amendments to the Specification begin on page 2 of this paper.

Amendments to the Claims are reflected in the listing of claims which begins on page 3 of this paper.

Remarks/Arguments begin on page 9 of this paper.

Appl. No. 11/410,699
Response dated July 3, 2007
Reply to Office Action of April 3, 2007

Amendments to the Specification:

Please paragraph [0016] with the following amended paragraph:

[0016] Referring to FIGURES 2 and 5, and each multichip module 102 may include a plurality of micro-electromechanical switches 104, which are also ~~referred~~ referred to as MEMs 104, between a first set of connectors 106 to the tester and a second set of connectors 108 to the plurality of devices under test. Each multichip module may include at least one driver 110 to selectively operate each of the plurality of micro-electromechanical switches 104.

Please paragraph [0016] with the following amended paragraph:

[0022] As MEM MCM 102 may be attached to probe card 112 using screws 120 or other fasteners, a new tester does not need to be purchased from a supplier of the ATE system. A customer may simply design a probe ~~card~~ card and attach these MEM MCMs to the probe card and install this new probe card assembly onto an existing ATE system.

Appl. No. 11/410,699
Response dated July 3, 2007
Reply to Office Action of April 3, 2007

Amendments to the Claims:

This listing of claims will replace all prior versions, and listing, of claims in the application:

Listing of Claims:

1. (Withdrawn) Apparatus for processing signals between a tester and a plurality of devices under test, the apparatus comprising:

 at least one multichip module, each of the at least one multichip module comprising:

 a plurality of micro-electromechanical switches between a first set of connectors to the tester and a second set of connectors to the plurality of devices under test; and

 at least one driver to selectively operate each of the plurality of micro-electromechanical switches.
2. (Withdrawn) Apparatus in accordance with claim 1, further comprising a probe card on which each one of the at least one multichip module is directly mounted.
3. (Withdrawn) Apparatus in accordance with claim 1, further comprising a plurality of MEMs dice on which the plurality of micro-electromechanical switches are formed.

Appl. No. 11/410,699
Response dated July 3, 2007
Reply to Office Action of April 3, 2007

4. (Withdrawn) Apparatus in accordance with claim 1, wherein the separate MEMs dice each include eight single pole triple throw switches.

5. (Withdrawn) Apparatus in accordance with claim 1, further comprising an attachment component for each one of the at least one multichip module, and wherein the attachment component mounts the multichip module to a probe card.

6. (Withdrawn) Apparatus in accordance with claim 5, wherein the attachment component includes passageways through the multichip module for a set of screws to mount the multichip module to the probe card.

7. (Withdrawn) Apparatus in accordance with claim 1, wherein the driver is designed to supply an electrostatic potential to activate a MEMs gate associated with each of the plurality of micro-electromechanical switches.

8. (Withdrawn) Apparatus in accordance with claim 1, wherein the at least one driver comprises a vacuum-florescent display driver dice.

9. (Withdrawn) A system for processing signals between a tester and a plurality of devices under test, the system comprising:

at least one multichip module mounted directly on a probe card and operable at a temperature of at least 125° C, and each of the at least one multichip module having a plurality of micro-electromechanical switches between a first set of

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connectors to the tester and a second set of connectors to the plurality of devices under test.

10. (Withdrawn) A system in accordance with claim 9, wherein the second set of connectors attach to a probe array having at least 6000 probe tip needles so as to test at least 6000 test sites of the plurality of devices under test during a single touchdown of the probe array.

11. (Withdrawn) A system for testing a plurality of devices under test, the system comprising:

a set of tester electronics to generate signals for application to the plurality of devices under test, and to receive signals generated by the plurality of devices under test;

a probe card with at least one multichip module mounted thereon, each of the at least one multichip module comprising a plurality of micro-electromechanical switches between a first set of connectors to the set of tester electronics and a second set of connectors to the plurality of devices under test, and a driver to selectively operate each of the plurality of micro-electromechanical switches; and

a probe array to transmit signals between the at least one multichip module of the probe card and the plurality of devices under test.

12. (Withdrawn) A system in accordance with claim 11, wherein each of the at least one multichip modules has a plurality of MEMS dice thereon.

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13. (Withdrawn) A system in accordance with claim 11, wherein each one of the plurality of MEMS dice each contain a plurality of micro-electromechanical switches.

14. (Withdrawn) A system in accordance with claim 13, wherein the switches are single pole triple throw switches.

15. (Withdrawn) A system in accordance with claim 13, wherein the switches are single pole double throw switches.

16. (Withdrawn) A system in accordance with claim 11, wherein the probe card has a maximum diameter of 440 millimeters.

17. (Withdrawn) A system in accordance with claim 16, wherein the probe card forms an opening for the probe array, and the opening has a minimum diameter of 330 millimeters.

18. (Withdrawn) A system in accordance with claim 11, wherein the probe array has at least 6000 probe tip needles so as to test at least 6000 test sites of the plurality of devices under test during a single touchdown of the probe array.

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19. (Amended) A method of processing signals between a tester and a plurality of devices under test, the method comprising:

connecting the tester and the plurality of devices under test with at least one multichip module, each of the at least one multichip module having a plurality of micro-electromechanical switches between a first set of connectors to the tester and a second set of connectors to the plurality of devices under test; and

selectively operating each of the plurality of micro-electromechanical switches to process the signals between individual ones of the first set of connectors to the tester and selected multiple ones of the second set of connectors to the plurality of devices under test.

20. (Original) A method in accordance with claim 19, further comprising operating the at least one multichip module at a speed of at least 100 MHz.

21. (Original) A method in accordance with claim 19, further comprising operating the multichip module at a temperature of at least 125° C.

22. (Original) A method in accordance with claim 19, further comprising mounting each of the at least one multichip module directly on the probe card.

23. (Original) A method in accordance with claim 19, further comprising mounting each of the at least one multichip module directly on the probe card,

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operating the multichip module at a temperature of at least 125° C, and operating the
at least one multichip module at a speed of at least 100 MHz.

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REMARKS/ARGUMENTS

Claims 1-23 remain in this application. Claim 19 has now been amended, without introducing new matter. Paragraphs [0016] and [0022] have been amended to correct minor typographical errors.

1. Restriction Requirement

Applicants affirm the election of claims 19-23 previously made on March 3, 2007.

2. Rejection of Claims 19-23 Under 35 U.S.C. 101

Claims 19-23 stand rejected under 35 U.S.C. 101 because the claimed invention is drawn to non-statutory subject matter.

In response, Applicants have now amended independent claim 19 to call for a method of processing signals between a tester and a plurality of devices under test, the method comprising connecting the tester and the plurality of devices under test with at least one multichip module, each of the at least one multichip module having a plurality of micro-electromechanical switches between a first set of connectors to the tester and a second set of connectors to the plurality of devices under test, and selectively operating each of the plurality of micro-electromechanical switches to process the signals between individual ones of the first set of connectors to the tester and selected multiple ones of the second set of connectors to the plurality of devices under test.

Applicants submit that connecting a tester and a plurality of devices under test with at least one multichip module, and selectively operating each of the plurality of micro-electromechanical switches to process the signals between individual ones of

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the first set of connectors to the tester and selected multiple ones of the second set of connectors to the plurality of devices under test produces a useful, concrete and tangible result. In other words, the present invention as claimed provides a method of processing signals between a tester and a plurality of devices under test by multiplexing connectors to the tester with connectors to the plurality of the devices under test. Accordingly, claim 19 is believed to be allowable.

Claims 20-23, which each depend directly from independent claim 19, are believed to be allowable for at least the same reasons as claim 19.

3. Rejection of Claims 19 and 22 Under 35 U.S.C. 103(a)

Claims 19 and 22 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Eldridge et al. (U.S. Patent No. 6,657,455; referred to herein as "Eldridge".)

Claim 19, as amended, calls for a method of processing signals between a tester and a plurality of devices under test, the method comprising connecting the tester and the plurality of devices under test with at least one multichip module, each of the at least one multichip module having a plurality of micro-electromechanical switches between a first set of connectors to the tester and a second set of connectors to the plurality of devices under test, and selectively operating each of the plurality of micro-electromechanical switches to process the signals between individual ones of the first set of connectors to the tester and selected multiple ones of the second set of connectors to the plurality of devices under test.

Eldridge does not teach or suggest selectively operating micro-mechanical switches to process signals between individual ones of connectors to a tester and selected multiple ones of connectors to a plurality of devices under test. Eldridge teaches away from the present invention inasmuch as the switches are transistor switches, and these transistor switches are disposed between devices under test and a power supply (rather than between a tester and devices under test). In addition, the specification of the present invention discloses that micro-electromechanical switches when compared to other switches have advantageous properties such as

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lower cost, higher reliability, and higher temperature operation. Accordingly, claim 19 is believed to be allowable.

Claim 22, which depends directly from independent claim 19, is believed to be allowable for at least the same reasons as claim 19.

4. Rejection of Claims 20, 21 and 23 Under 35 U.S.C. 103(a)

Claims 20, 21 and 23 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Eldridge in view of McCord (U.S. Patent No. 6,681,869; referred to herein as "McCord") in view of Akram (U.S. Patent No. 6,640,323; referred to herein as "Akram")

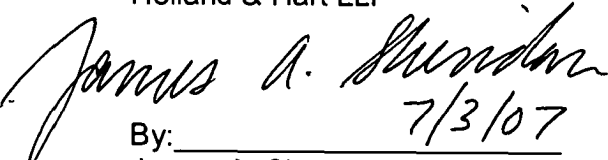
Claims 20, 21 and 23 each depend directly from independent claim 19. As discussed above, Eldridge teaches away from the present invention of claim 19. Furthermore, neither McCord nor Akram teach or suggest a method of processing signals between a tester and a plurality of devices under test which includes selectively operating micro-mechanical switches to process signals between individual ones of connectors to a tester and selected multiple ones of connectors to a plurality of devices under test. Accordingly, claims 20, 21 and 23 are believed to be allowable for at least the same reason as claim 19.

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Conclusion

In light of the amendments and remarks provided herein, Applicants respectfully request the timely issuance of a Notice of Allowance.

Respectfully submitted,
Holland & Hart LLP


By: James A. Sheridan 7/3/07

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PTO/SB/06 (08-03)

Approved for use through 7/31/2006. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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PATENT APPLICATION FEE DETERMINATION RECORD						Application or Docket Number 11410699	
Substitute for Form PTO-875							
CLAIMS AS FILED – PART I							
(Column 1)		(Column 2)		(Column 3)			
FOR	NUMBER FILED	NUMBER EXTRA					
BASIC FEE (37 CFR 1.16(a))							
TOTAL CLAIMS (37 CFR 1.16(c))	minus 20 =		*				
INDEPENDENT CLAIMS (37 CFR 1.16(b))	minus 3 =		*				
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(d))							
* If the difference in column 1 is less than zero, enter "0" in column 2.							
CLAIMS AS AMENDED – PART II							
(Column 1)		(Column 2)		(Column 3)			
AMENDMENT A	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA				
	Total (37 CFR 1.16(c))	*	Minus	**	=		
	Independent (37 CFR 1.16(b))	*	Minus	***	=		
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(d))						
(Column 1)		(Column 2)		(Column 3)			
AMENDMENT B	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA				
	Total (37 CFR 1.16(c))	*	Minus	**	=		
	Independent (37 CFR 1.16(b))	*	Minus	***	=		
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(d))						
(Column 1)		(Column 2)		(Column 3)			
AMENDMENT C	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA				
	Total (37 CFR 1.16(c))	*	Minus	**	=		
	Independent (37 CFR 1.16(b))	*	Minus	***	=		
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(d))						
• If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.							

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	457	324/754-765.ccls. and switch with prob\$4 and (DUT or device or chip or unit or component) with test\$4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2007/09/24 13:21
L2	192	1 and probe with card	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2007/09/24 13:22
L3	177	2 not agilent	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2007/09/24 13:22
L4	33	(electromechanical or means) same prob\$4 with (card or module or apparatus) and 324/754.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2007/09/24 13:23
L7	38	("4144536" "5101149" "5422562" "5502671" "5721495" "5760599" "5822166").PN. OR ("6339338").URPN.	US-PGPUB; USPAT; USOCR	ADJ	ON	2007/09/24 13:25
L8	31	("3676777" "3895297" "4631724" "4712058" "4746855" "4849691" "5025344" "5032789" "5057774" "5101149" "5101151" "5101153" "5146161" "5294883" "5371457" "5392293" "5404099" "5406217" "5412315" "5414352").PN. OR ("5721495").URPN.	US-PGPUB; USPAT; USOCR	ADJ	ON	2007/09/24 13:25
L9	27	("4336495" "4398146" "4628253" "4714876" "4733168" "4779041" "4967151" "4970454" "5012185" "5019772" "5030904").PN. OR ("5294883").URPN.	US-PGPUB; USPAT; USOCR	ADJ	ON	2007/09/24 13:26
L10	177	2 not agilent	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2007/09/24 13:27

EAST Search History

L11	174	3 and (test\$4 with (device or system or apparatus))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2007/09/24 13:29
L14	48	324/754-765 and (test\$4) same prob\$4 and (test\$4 with (device or system or apparatus))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2007/09/24 13:31
S1	12	324/415.ccls. and probe	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2007/09/18 11:32
S2	2	324/168,180.ccls. and probe	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2007/09/18 11:32
S3	1	324/168,180.ccls. and dut	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2007/09/18 11:32
S4	318	324/168,180.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2007/09/18 11:33
S5	52	324/754.ccls. and switch with probe adj card	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2007/09/18 11:47
S6	105	324/754-765.ccls. and switch with probe adj card	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2007/09/24 13:20

EAST Search History

S7	101	S6 not agilent	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2007/09/18 14:24
S8	102630	electromechanical	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2007/09/18 14:24
S9	105	electromechanical with switch\$2 same probe	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2007/09/18 14:24
S10	105	S9 not agilent	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2007/09/18 14:25
S11	75	S9 and @py<"2004"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2007/09/18 14:25
S12	50	("3493858" "4500836" "4517512" "5055780" "5070297" "5506510").PN. OR ("5736850"). URPN.	US-PGPUB; USPAT; USOCR	ADJ	ON	2007/09/18 15:00
S13	868	mccord.in.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2007/09/18 15:08
S14	0	S13 amd tester	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2007/09/18 15:08

EAST Search History

S15	7	S13 and tester	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2007/09/18 15:09
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/410,699	04/24/2006	Romi Mayder	10060220-1	4586
63448 VERIGY 4700 INNOVATION WAY, BLDG D1 FORT COLLINS, CO 80528	7590 09/27/2007		EXAMINER ISLA RODAS, RICHARD	
			ART UNIT 2829	PAPER NUMBER
			MAIL DATE 09/27/2007	DELIVERY MODE PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

11/410,699

Applicant(s)

MAYDER ET AL.

Examiner

Richard Isla-Rodas

Art Unit

2829

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 06 July 2007.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-23 is/are pending in the application.
- 4a) Of the above claim(s) 1-18 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 19-23 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 24 April 2006 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

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DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claim 19 have been considered but are moot in view of the new ground(s) of rejection.

Claim Objections

2. Claims 22 and 23 are objected to because of the following informalities:

Claims 22 and 23 recite the limitation "the probe card" in line 2 of each claim. It appears that it should be "a probe card".

Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 19 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over the US Patent to Legal (5,736,850) in view of the US Patent to Leggett et al. 6,098,142 (Leggett hereinafter).

In terms of claims 19 and 22, legal teaches in Figure 2A, a method of processing signal between a tester (110) and a plurality of devices under test (cells on top of wafer

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122), with at least one multichip module (216) mounted directly on a probe card (218), the module having a plurality of mechanical switches (see lines 59-61 in column 4) between a first set of connectors (DRIVER/RECEIVERS) to the tester (110) and a second set of connectors (220) to the plurality of devices under test (cells on wafer 122), and selectively operating each of the plurality of mechanical switches to process (receive and transmit) the signals between individual ones of the first set of connector to the tester and selected multiple ones of the second set of connectors to the plurality of devices under test (The relays provide independent conductive paths between the tester and the probes, said relays can be actuated to connect one of the group of drivers to one of the test sites as explained in lines 50-58, column 4). Legal, teaches that the mechanical switches may also be switches that have control inputs (electrical) or a similar structure (see lines 61-64 in column 4). Legal however, does not explicitly state the use of micro electro-mechanical switches. Nevertheless, it has been held that to be entitled weight in method claims, the recited-structure limitations therein (electro-mechanical switch) must affect the method in a manipulative sense, and not to amount to the mere claiming of a use of a particular structure (in the immediate case, the preferred use of electro-mechanical switches). Ex parte Pfeiffer, 1962 C.D. 408 (1961).

Furthermore, the use of electromechanical switches as preferred structures would have been well known to someone in the art at the time of the invention, as evidenced by Leggett. Leggett, teaches in lines 26-30 of column 3, that electromechanical switches can be used as switches for transmission. Therefore, because these two switches (mechanical and electromechanical) were art-recognized

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equivalents at the time the invention was made, one of ordinary skill in the art would have found it obvious to substitute mechanical for electro-mechanical.

5. Claims 20, 21 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Legal in view of Leggett, further in view of the US Patent to McCord 6,681,869 (McCord hereinafter) and further in view of the US Patent to Akram 6,640,323.

As to claims 20, 21 and 23, Legal in view of Leggett substantially teaches all of the claimed steps as discussed above including mounting the multichip module (216) directly on a probe card (218). Legal in view of Leggett does not explicitly teach however, the step of operating the multichip module at a speed (frequency) of at least 100 MHz. McCord shows that it's well known in the art that to operate a tester (and consequently the module connecting it to the device under test) at and above the rated clock frequency of the device under test (see lines 29-38 in column 10). For instance, when testing a device which working frequency is 533 MHz, is customary to process the signals at frequencies up to 584MHz. It would have been obvious to one of ordinary skill in the art, to operate the multichip module at 100MHz or more when testing devices whose frequency of operation is below such frequency, as taught by McCord, in order to replicate the working conditions of said devices. Furthermore, Legal in view of McCord is silent as to the preferred temperature of operation of the device. Akram teaches a procedure known as static method of burn-in that consists of applying test signals on devices under test at temperatures of 125 degrees Celsius. Such method comprises the step of applying operating voltages on the devices under test that are much higher

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than their normal operating voltage, thereby increasing the temperature of the devices under test and removing those devices that fail to withstand the temperature and/or voltage (infant mortality of dies), as explained in lines 21-32 in column 2. It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to apply higher than normal operating voltages on the devices under test (by operating the multichip module to send higher than normal test signals to the devices under test) thereby increasing the temperature of operation to up to 125 degrees, as taught by Akram, in order to detect early failure of the devices under test (infant mortality of dies) as suggested by Akram in line 10 of column 2.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. US Patents to Granicher et al. (7,245,134) and Roy et al. (6,678,850).

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

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shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Richard Isla-Rodas whose telephone number is (571) 272-5056. The examiner can normally be reached on Monday through Friday 8 am to 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ha Nguyen can be reached on (571) 272-1678. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Richard Isla-Rodas
September 18, 2007


HA TRAN NGUYEN
SUPERVISORY PATENT EXAMINER

Notice of References Cited

Application/Control No.

11/410,699

Applicant(s)/Patent Under
Reexamination
MAYDER ET AL.

Examiner

Richard Isla-Rodas

Art Unit

2829

Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-7,245,134	07-2007	Granicher et al.	324/754
*	B	US-6,678,850	01-2004	Roy et al.	714/730
*	C	US-6,098,142	08-2000	Leggett et al.	710/220
*	D	US-5,736,850	04-1998	Legal, Dennis Andrew	324/158.1
*	E	US-6,801,869	10-2004	McCord, Don	702/117
*	F	US-6,640,323	10-2003	Akram, Salman	714/724
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
 Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Figure 1

Figure 1 consists of two panels, (a) and (b), showing the evolution of the number of nodes (N) over time (t). Panel (a) shows the evolution of the number of nodes in the network, which starts at approximately 100 and increases rapidly, reaching a plateau around 1000 after about 100 time steps. The curve is smooth and follows a sigmoidal shape. Panel (b) shows the evolution of the number of nodes in the network, which starts at approximately 100 and increases rapidly, reaching a plateau around 1000 after about 100 time steps. The curve is smooth and follows a sigmoidal shape.

Richard Isla-Rodas

2829

[illegible]

INTERFERENCE SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES (INCLUDING SEARCH STRATEGY)		
	DATE	EXMR
EAST (US-PGPUB, USPAT, USOCR, EPO, JPO, DERWENT, IBM_T DB)- See Search History Printout	9/18/2007	RI
324/168,180.ccls. (text search only – see history print out)	9/18/2007	RI
324/415.ccls. (text search only – see history print out)	9/18/2007	RI



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APPLICATION NUMBER	FILING OR 371(c) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
11/410,699	04/24/2006	Romi Mayder	10060220-1

CONFIRMATION NO. 4586

63448
VERIGY
4700 INNOVATION WAY, BLDG D1
FORT COLLINS, CO80528

Title: Apparatus, systems and methods for processing signals between a tester and a plurality of devices under test at high temperatures and with single touchdown of a probe array

Publication No. US-2007-0247140-A1

Publication Date: 10/25/2007

NOTICE OF PUBLICATION OF APPLICATION

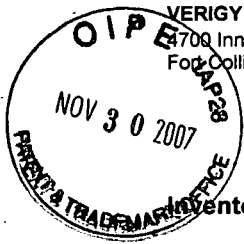
The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publicly available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently <http://www.uspto.gov/patft/>.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Office of Public Records. The Office of Public Records can be reached by telephone at (703) 308-9726 or (800) 972-6382, by facsimile at (703) 305-8759, by mail addressed to the United States Patent and Trademark Office, Office of Public Records, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently <http://pair.uspto.gov/>. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.



ATTORNEY DOCKET NO. 10060220-1

AF/IFW

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Romi Mayder, et al.

Serial No.: 11/410,699

Examiner: Richard Isla Rodas

Filing Date: April 24, 2006

Group Art Unit: 2829

Title: APPARATUS, SYSTEMS AND METHODS FOR PROCESSING SIGNALS BETWEEN A TESTER AND A PLURALITY OF DEVICES UNDER TEST AT HIGH TEMPERATURES AND WITH SINGLE TOUCHDOWN OF A PROBE ARRAY

COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria VA 22313-1450

TRANSMITTAL LETTER FOR RESPONSE/AMENDMENT

Sir:

Transmitted herewith is/are the following in the above-identified application:

- ☒ Response/Amendment ☐ Petition to extend time to respond
☐ New fee as calculated below ☐ Supplemental Declaration
☒ No additional fee (Address envelope to "Mail Stop Amendments")
☐ Other: (Fee \$____)

CLAIMS AS AMENDED BY OTHER THAN A SMALL ENTITY						
(1) FOR	(2) CLAIMS REMAINING AFTER AMENDMENT	(3) NUMBER EXTRA	(4) HIGHEST NUMBER PREVIOUSLY PAID FOR	(5) PRESENT EXTRA	(6) RATE	(7) ADDITIONAL FEES
TOTAL CLAIMS	23	MINUS	23	= 0	X 50	\$ 0
INDEP. CLAIMS	4	MINUS	4	= 0	X 200	\$ 0
<input type="checkbox"/> FIRST PRESENTATION OF A MULTIPLE DEPENDENT CLAIM					+ 360	\$ 0
EXTENSION FEE	1 ST MONTH 120.00 <input type="checkbox"/>	2 ND MONTH 450.00 <input type="checkbox"/>	3 RD MONTH 1020.00 <input type="checkbox"/>	4 TH MONTH 1590.00 <input type="checkbox"/>		\$ 0
OTHER FEES						\$ 0
TOTAL ADDITIONAL FEE FOR THIS AMENDMENT						\$ 0

Charge \$0 to Deposit Account 08-2623. At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account 08-2623 pursuant to 37 CFR 1.2 5. Additionally please charge any fees to Deposit Account 08-2623 under 37 CFR 1.16, 1.17, 1.19, 1.20 and 1.21. A duplicate copy of this transmittal letter is enclosed.

Respectfully submitted,

Romi Mayder, et al.

By

Gregory W. Osterloth
Attorney/Agent for Applicant(s)

I hereby certify that this correspondence is being Deposited with the United States Postal Service as First class mail in an envelope addressed to: Commissioner for Patents, PO Box 1450, Alexandria, VA 22313-1450.

Date of Deposit: November 27, 2007

Typed Name: Gregory W. Osterloth

Signature:

Reg. No. 36,232

Date: November 27, 2007

Telephone No. (303) 295-8205



**Reply under 37 CFR 1.116 –
Expedited Procedure –
Technology Center 2800**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appl. No.	:	11/410,699	Confirmation No. 4586
Applicant	:	Romi Mayder, et al.	
Filed	:	04/24/2006	
TC/A.U.	:	2829	
Examiner	:	Isla Rodas, Richard	
Docket No.	:	10060220-1	

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

REPLY UNDER 37 CFR 1.116 – EXPEDITED PROCEDURE

Sir:

In response to the Final Office Action of September 27, 2007, please amend the above-identified application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks/Arguments begin on page 6 of this paper.

Appl. No. 11/410,699
Reply dated Nov. 27, 2007
Reply to Final Office Action of Sep. 27, 2007

Amendments to the Claims:

This listing of claims will replace all prior versions, and listing, of claims in the application:

Listing of Claims:

1. (Withdrawn) Apparatus for processing signals between a tester and a plurality of devices under test, the apparatus comprising:
 - at least one multichip module, each of the at least one multichip module comprising:
 - a plurality of micro-electromechanical switches between a first set of connectors to the tester and a second set of connectors to the plurality of devices under test; and
 - at least one driver to selectively operate each of the plurality of micro-electromechanical switches.
2. (Withdrawn) Apparatus in accordance with claim 1, further comprising a probe card on which each one of the at least one multichip module is directly mounted.
3. (Withdrawn) Apparatus in accordance with claim 1, further comprising a plurality of MEMs dice on which the plurality of micro-electromechanical switches are formed.
4. (Withdrawn) Apparatus in accordance with claim 1, wherein the separate MEMs dice each include eight single pole triple throw switches.
5. (Withdrawn) Apparatus in accordance with claim 1, further comprising an attachment component for each one of the at least one multichip module, and wherein the attachment component mounts the multichip module to a probe card.

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6. (Withdrawn) Apparatus in accordance with claim 5, wherein the attachment component includes passageways through the multichip module for a set of screws to mount the multichip module to the probe card.

7. (Withdrawn) Apparatus in accordance with claim 1, wherein the driver is designed to supply an electrostatic potential to activate a MEMs gate associated with each of the plurality of micro-electromechanical switches.

8. (Withdrawn) Apparatus in accordance with claim 1, wherein the at least one driver comprises a vacuum-florescent display driver dice.

9. (Withdrawn) A system for processing signals between a tester and a plurality of devices under test, the system comprising:

at least one multichip module mounted directly on a probe card and operable at a temperature of at least 125° C, and each of the at least one multichip module having a plurality of micro-electromechanical switches between a first set of connectors to the tester and a second set of connectors to the plurality of devices under test.

10. (Withdrawn) A system in accordance with claim 9, wherein the second set of connectors attach to a probe array having at least 6000 probe tip needles so as to test at least 6000 test sites of the plurality of devices under test during a single touchdown of the probe array.

11. (Withdrawn) A system for testing a plurality of devices under test, the system comprising:

a set of tester electronics to generate signals for application to the plurality of devices under test, and to receive signals generated by the plurality of devices under test;

a probe card with at least one multichip module mounted thereon, each of the at least one multichip module comprising a plurality of micro-electromechanical switches

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between a first set of connectors to the set of tester electronics and a second set of connectors to the plurality of devices under test, and a driver to selectively operate each of the plurality of micro-electromechanical switches; and

a probe array to transmit signals between the at least one multichip module of the probe card and the plurality of devices under test.

12. (Withdrawn) A system in accordance with claim 11, wherein each of the at least one multichip modules has a plurality of MEMS dice thereon.

13. (Withdrawn) A system in accordance with claim 11, wherein each one of the plurality of MEMS dice each contain a plurality of micro-electromechanical switches.

14. (Withdrawn) A system in accordance with claim 13, wherein the switches are single pole triple throw switches.

15. (Withdrawn) A system in accordance with claim 13, wherein the switches are single pole double throw switches.

16. (Withdrawn) A system in accordance with claim 11, wherein the probe card has a maximum diameter of 440 millimeters.

17. (Withdrawn) A system in accordance with claim 16, wherein the probe card forms an opening for the probe array, and the opening has a minimum diameter of 330 millimeters.

18. (Withdrawn) A system in accordance with claim 11, wherein the probe array has at least 6000 probe tip needles so as to test at least 6000 test sites of the plurality of devices under test during a single touchdown of the probe array.

19. (Previously Presented) A method of processing signals between a tester and a plurality of devices under test, the method comprising:

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connecting the tester and the plurality of devices under test with at least one multichip module, each of the at least one multichip module having a plurality of micro-electromechanical switches between a first set of connectors to the tester and a second set of connectors to the plurality of devices under test; and

selectively operating each of the plurality of micro-electromechanical switches to process the signals between individual ones of the first set of connectors to the tester and selected multiple ones of the second set of connectors to the plurality of devices under test.

20. (Original) A method in accordance with claim 19, further comprising operating the at least one multichip module at a speed of at least 100 MHz.

21. (Original) A method in accordance with claim 19, further comprising operating the multichip module at a temperature of at least 125° C.

22. (Currently Amended) A method in accordance with claim 19, further comprising mounting each of the at least one multichip module directly on ~~[[the]]~~a probe card.

23. (Currently Amended) A method in accordance with claim 19, further comprising mounting each of the at least one multichip module directly on ~~[[the]]~~a probe card, operating the multichip module at a temperature of at least 125° C, and operating the at least one multichip module at a speed of at least 100 MHz.

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Reply to Final Office Action of Sep. 27, 2007

REMARKS/ARGUMENTS

Claims 1-23 remain in this application. Of these, claims 19-23 stand rejected, and claims 1-18 stand withdrawn. Claims 22 and 23 also stand objected to.

1. Objection of Claims 22 and 23

Claims 22 and 23 stand objected to because "the probe card" should be --a probe card--. Appropriate corrections have been made.

2. Rejection of Claims 19 and 22 Under 35 USC 103(a)

Claims 19 and 22 stand rejected under 35 USC 103(a) as being unpatentable over Legal (U.S. Pat. No. 5,736,850) in view of Leggett et al. (U.S. Pat. No. 6,098,142; hereinafter referred to as "Leggett").

With respect to claim 19, the Examiner asserts that Legal discloses connecting a tester and a plurality of devices under test with "at least one multichip module (216). . . (see lines 59-61 in column 4)". See, 9/27/2007 Final Office Action, p. 3, sec. 4. However, nowhere does Legal indicate that the "relay matrix 216" is, or includes, a multichip module. Column 4, lines 59-61, of Legal state:

Relays 312 may be traditional mechanical type relays. Alternatively, they could be solid state switches or other similar structure.

However, there is no mention that the relay matrix 216 is or should be implemented using a multichip module, or that the tester 110 should be connected to devices under test via switches on a multichip module.

The Examiner further states, with respect to claim 19, that:

. . . Legal, teaches that the mechanical switches may also be switches that have control inputs (electrical) or a similar structure (see lines 61-64 in column 4).

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Reply dated Nov. 27, 2007
Reply to Final Office Action of Sep. 27, 2007

Legal however, does not explicitly state the use of micro electro-mechanical switches. Nevertheless, it has been held that to be entitled weight in method claims, the recited-structure limitations therein (electro-mechanical switch) must affect the method in a manipulative sense, and not to amount to the mere claiming of a use of a particular structure (in the immediate case, the preferred use of electro-mechanical switches). *Ex parte Pfeiffer*, 1962 C.D. 408 (1961).

9/27/2007 Final Office Action, p. 3., sec. 4.

To begin, applicants note that the switches mentioned in their claim 19 are "micro-electromechanical switches" (MEMS), and the MEMS are provided on a "multichip module". Not only does Legal fail to disclose or suggest the use of MEMS to connect a tester with devices under test, but Legal also fails to disclose or suggest the use of MEMS on at least one multichip module. As mentioned in applicants' specification, MEMS on multichip modules may be switched at faster speeds and used at higher temperatures.

Although the Examiner relies on *Ex parte Pfeiffer*, applicants note that the Board has consistently refused to apply any *per se rule* in addressing 35 USC 103 rejections - even in the context of method claims. At times, the Board has cited to *In re Ochiai*, which holds:

The use of *per se* rules, while undoubtedly less abhorious than a searching comparison of the claimed invention - including all its limitations - with the teachings of the prior art, flouts section 103 and the fundamental case law applying it. *Per se* rules that eliminate the need for fact-specific analysis of claims and prior art may be administratively convenient for PTO Examiners and the Board. Indeed, they have been sanctioned by the Board as well. But reliance on *per se* rules of obviousness is legally incorrect and must cease. Any such administrative convenience is simply inconsistent with section 103, which, according to *Graham [v. John Deere Co.]*, 383 U.S. 1, 148 USPQ 459 (1966)] and its progeny, entitles an applicant to issuance of an otherwise proper patent unless the PTO established that the invention as claimed in the application is obvious over cited prior art, based on the specific comparison of that prior art with claim limitations.

In re Ochiai, 71 F.3d at 1572, 37 USPQ2d at 1133.

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Although the Examiner relies on Leggett's teachings for the proposition that mechanical and electromechanical switches are equivalent, Leggett, like Legal, fails to disclose either MEMS or microchip modules.

Given that neither Legal nor Leggett teach or suggest "connecting [a] tester and [a] plurality of devices under test ***with at least one multichip module, each of the at least one multichip module having a plurality of micro-electromechanical switches***", applicants believe claim 19 to be allowable.

Claim 22 is believed to be allowable because it depends from claim 19, and because Legal and Leggett fail to teach or suggest "mounting each of the at least one multichip module directly on a probe card" (i.e., because neither reference discloses a multichip module or discusses where or how such a module would be used or mounted).

3. Rejection of Claims 20, 21 and 23 Under 35 USC 103(a)

Claims 20, 21 and 23 stand rejected under 35 USC 103(a) as being unpatentable over Legal (U.S. Pat. No. 5,736,850) in view of Leggett et al. (U.S. Pat. No. 6,098,142; hereinafter referred to as "Leggett"), McCord (U.S. Pat. No. 6,681,869) and Akram (U.S. Pat. No. 6,640,323).


Claims 20, 21 and 23 are believed to be allowable, at least, because each of these claims depends from claim 19, and because McCord and Akram fail to disclose that which is missing from the combined teachings of Legal and Leggett. See, e.g., the discussion of Legal and Leggett in Section 2 of these Remarks/Arguments.

Appl. No. 11/410,699
Reply dated Nov. 27, 2007
Reply to Final Office Action of Sep. 27, 2007

4. Conclusion

In light of the amendments and remarks provided herein, Applicants respectfully request the timely issuance of a Notice of Allowance.

Respectfully submitted,
HOLLAND & HART, LLP

By: 

Gregory W. Osterloth
Reg. No. 36,232
Tel: (303) 295-8205

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875					Application or Docket Number 11/410,699		Filing Date 04/24/2006		<input type="checkbox"/> To be Mailed				
APPLICATION AS FILED – PART I													
(Column 1)			(Column 2)			SMALL ENTITY <input type="checkbox"/> OR		OTHER THAN SMALL ENTITY					
FOR		NUMBER FILED		NUMBER EXTRA		RATE (\$)		FEE (\$)					
<input type="checkbox"/> BASIC FEE (37 CFR 1.16(a), (b), or (c))		N/A		N/A		N/A							
<input type="checkbox"/> SEARCH FEE (37 CFR 1.16(k), (l), or (m))		N/A		N/A		N/A							
<input type="checkbox"/> EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))		N/A		N/A		N/A							
TOTAL CLAIMS (37 CFR 1.16(i))		23 minus 20 =		* 3		X \$ =				OR X \$50 =			
INDEPENDENT CLAIMS (37 CFR 1.16(h))		4 minus 3 =		* 1		X \$ =				OR X \$200 =			
<input type="checkbox"/> APPLICATION SIZE FEE (37 CFR 1.16(s))		If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).											
<input type="checkbox"/> MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))													
* If the difference in column 1 is less than zero, enter "0" in column 2.													
TOTAL						TOTAL 350							
APPLICATION AS AMENDED – PART II													
(Column 1)			(Column 2)			(Column 3)			SMALL ENTITY OR		OTHER THAN SMALL ENTITY		
AMENDMENT	11/30/2007		CLAIMS REMAINING AFTER AMENDMENT				HIGHEST NUMBER PREVIOUSLY PAID FOR		PRESENT EXTRA				
	Total (37 CFR 1.16(i))		* 23		Minus		** 23		= 0				
	Independent (37 CFR 1.16(h))		* 4		Minus		*** 4		= 0				
	<input type="checkbox"/> Application Size Fee (37 CFR 1.16(s))												
	<input type="checkbox"/> FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))												
	TOTAL ADD'L FEE											OR TOTAL ADD'L FEE 0	
AMENDMENT			CLAIMS REMAINING AFTER AMENDMENT				HIGHEST NUMBER PREVIOUSLY PAID FOR		PRESENT EXTRA				
	Total (37 CFR 1.16(i))		*		Minus		**		=				
	Independent (37 CFR 1.16(h))		*		Minus		***		=				
	<input type="checkbox"/> Application Size Fee (37 CFR 1.16(s))												
	<input type="checkbox"/> FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))												
	TOTAL ADD'L FEE											OR TOTAL ADD'L FEE	
<p>* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.</p> <p>** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".</p> <p>*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".</p> <p>The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.</p>													

Legal Instrument Examiner:
/GERALDINE STANLEY/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/410,699	04/24/2006	Romi Mayder	10060220-1	4586
63448	7590	12/27/2007		
VERIGY 4700 INNOVATION WAY, BLDG D1 FORT COLLINS, CO 80528			EXAMINER ISLA RODAS, RICHARD	
			ART UNIT 2829	PAPER NUMBER
			MAIL DATE 12/27/2007	DELIVERY MODE PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Advisory Action **Before the Filing of an Appeal Brief**

Application No.

11/410,699

Applicant(s)

MAYDER ET AL.

Examiner

Richard Isla-Rodas

Art Unit

2829

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 30 November 2007 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

1. ☒ The reply was filed after a final rejection, but prior to or on the same day as filing a Notice of Appeal. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. The reply must be filed within one of the following time periods:

- a) ☒ The period for reply expires 3 months from the mailing date of the final rejection.
b) ☐ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.

Examiner Note: If box 1 is checked, check either box (a) or (b). ONLY CHECK BOX (b) WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

AMENDMENTS

3. ☐ The proposed amendment(s) filed after a final rejection, but prior to the date of filing a brief, will not be entered because:
- (a) ☐ They raise new issues that would require further consideration and/or search (see NOTE below);
(b) ☐ They raise the issue of new matter (see NOTE below);
(c) ☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
(d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.

NOTE: _____. (See 37 CFR 1.116 and 41.33(a)).

4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).
5. ☒ Applicant's reply has overcome the following rejection(s): See Continuation Sheet.
6. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
7. ☒ For purposes of appeal, the proposed amendment(s): a) ☐ will not be entered, or b) ☒ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.
The status of the claim(s) is (or will be) as follows:
Claim(s) allowed: _____
Claim(s) objected to: _____
Claim(s) rejected: 19-23.
Claim(s) withdrawn from consideration: 1-18.

AFFIDAVIT OR OTHER EVIDENCE

8. ☐ The affidavit or other evidence filed after a final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).
9. ☐ The affidavit or other evidence filed after the date of filing a Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing of good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).
10. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

11. ☒ The request for reconsideration has been considered but does NOT place the application in condition for allowance because: See Continuation Sheet.
12. ☐ Note the attached Information Disclosure Statement(s). (PTO/SB/08) Paper No(s). _____
13. ☐ Other: _____

Continuation Sheet (PTO-303)

Application No. 11/410,699

Continuation of 5. Applicant's reply has overcome the following rejection(s): Objection to claims 22 and 23 as stated in page 2 of the Final Rejection.

Continuation of 11. does NOT place the application in condition for allowance because: The amendment to claims 22 and 23 overcome the objections for antecedent basis set up in page 2 of the Final Office Action.

In response to applicant's arguments that Legal does not teach MEMS that may be switched at faster speeds and used at higher temperatures.

- Firstly, applicant does not recite "MEMS". Applicant recites "micro-electromechanical switches". Given the broadest reasonable interpretation of the preferred structure the applicant uses to perform the method claim, the limitation recites a mechanical switch that is actuated electrically and which works on the micrometer scale. That is a small mechanical switch that may be operated/switched/actuated electrically. The prior art anticipates said limitation (see Final rejection pages 2-4)

- Secondly, the applicant does not state where in the specifications said mention that MEMS on multichip modules may be switched at faster speeds and used at higher temperatures is. Still, even if the specifications mentions said ability of the MEMS to switch at faster speeds or higher temperatures (which would also raise the question: higher than what? and faster than what?), applicant misinterprets the principle that claims are interpreted in the light of the specification. Although these virtues (speed or high temperature operability) may be found as examples or embodiments in the specification, they were not claimed explicitly. Nor were the words that are used in the claims defined in the specification, to require these limitations. A reading of the specification provides no evidence to indicate that these limitations must be imported into the claims to give meaning to disputed terms (Constant v. Advanced Micro-Devices Inc., 7 USPQ 2d 1064.).

Likewise, the recitation "multichip module" has been given its broadest reasonable interpretation as a module that is capable of connecting to a plurality of chips. As shown in Figure 3 of Legal, the module 216 indeed is capable of connecting to a plurality of device (310) and therefore is capable of connecting to a plurality of chips. It must be noted that this interpretation of "multichip module" was relied on in the preparation of the Non Final office action submitted 4/3/2007 (see lines 4-6 in paragraph 11 of page 5), which the applicant did not argued against.

In addition, the examiner disagrees with the contention that in the examination process, the examiner has used case law (Ex parte Pfeiffer) as a per se rule in order to make the examination process less laborious (see lines 1-3 in paragraph 3, page 7 of submitted Remarks). The examiner had considered all limitations and after determining that, the claimed preferred devices (micro-electromechanical switches) do not affect the method in a manipulative manner that differs from that which is accomplished by using the elements in the prior art of record (relays) the examiner determined that the sole use of said preferred structure could not distinguish the claimed method from the method disclosed by the prior art. The examiner did not simply dismiss the claims by applying a per se rule but rather used the available case law (Ex parte Pfeiffer) to support his rejection.


HA TRAN NGUYEN
SUPERVISORY PATENT EXAMINER



Reply under 37 CFR 1.116 –
Expedited Procedure –
Technology Center 2800

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appl. No. : 11/410,699
Applicant : Romi Mayder, et al.
Filed : 04/24/2006
TC/A.U. : 2829
Examiner : Isla Rodas, Richard

Confirmation No. 4586

Docket No. : 10060220-1

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

REPLY UNDER 37 CFR 1.116 – EXPEDITED PROCEDURE

Sir:

In response to the Final Office Action of September 27, 2007, please amend the above-identified application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks/Arguments begin on page 6 of this paper.

*Please enter after Final
Amendment.*

Thank you

R.I. 12/26/07

AF
D

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Romi Mayder, et al.

Serial No.: 11/410,699

Filing Date: April 24, 2006



Examiner: RICHARD ISLA RODAS

Group Art Unit: 2829

Title: APPARATUS, SYSTEMS AND METHODS FOR PROCESSING SIGNALS BETWEEN A TESTER AND A PLURALITY OF DEVICES UNDER TEST AT HIGH TEMPERATURES AND WITH SINGLE TOUCHDOWN OF A PROBE ARRAY

COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria VA 22313-1450

NOTICE OF APPEAL FROM THE EXAMINER TO THE
BOARD OF PATENT APPEALS AND INTERFERENCES

Sir:

Applicant hereby appeals to the Board of Patent Appeals and Interferences from the decision of the examiner dated, September 27, 2007, rejecting the following claims 19-23

The fee for this Notice of Appeal (37 CFR 1.17(b)) is \$510.00.

(complete (a) or (b) as applicable)

The proceedings herein are for a patent application and the provisions of 37 CFR 1.136(a) apply.

☒ (a) Applicant petitions for an extension of time under 37 CFR 1.136 (fees: 37 CFR 1.17(a)-(d) for the total number of months checked below:

<input checked="" type="checkbox"/>	one month	\$ 120.00
<input type="checkbox"/>	two months	\$ 460.00
<input type="checkbox"/>	three months	\$1050.00
<input type="checkbox"/>	four months	\$1640.00

02/01/2008 SDENB0B3 00000040 002623 11410699
01 FC:1401 510.00 DA
02 FC:1251 120.00 DA

☐ The extension fee has already been filled in this application.

☐ (b) Applicant believes that no extension of term is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

Please charge to Deposit Account **08-2623** the sum of \$630.00. At any time during the pendency of this application, please charge any fees required or credit any overpayment to Deposit Account **08-2623** pursuant to 37 CFR 1.25.

A duplicate copy of this transmittal letter is enclosed.

☒ I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Date of Deposit: January 28, 2008 OR

☐ I hereby certify that this paper is being facsimile transmitted to the Patent and Trademark Office on the date shown below.

Date of Facsimile:

Typed Name: Gregory W. Osterloth

Signature:

Respectfully submitted,
Romi Mayder, et al.

By

Gregory W. Osterloth
Attorney/Agent for Applicant(s)

Reg. No. 36,232

Date: January 28, 2008

Telephone No. (303) 295-8205

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Romi Mayder, et al.

Serial No.: 11/410,699

Filing Date: April 24, 2006

Examiner: Richard Isla Rodas

Group Art Unit: 2829



Title: APPARATUS, SYSTEMS AND METHODS FOR PROCESSING SIGNALS BETWEEN A TESTER AND A PLURALITY OF DEVICES UNDER TEST AT HIGH TEMPERATURES AND WITH SINGLE TOUCHDOWN OF A PROBE ARRAY

COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria VA 22313-1450

TRANSMITTAL OF APPEAL BRIEF

Sir:

Transmitted herewith is the Appeal Brief in this application with respect to the Notice of Appeal filed on January 28, 2008 (and received by the Office on February 1, 2008).

The fee for filing this Appeal Brief is (37 CFR 1.17(c)) **\$510.00**.

(complete (a) or (b) as applicable)

The proceedings herein are for a patent application and the provisions of 37 CFR 1.136(a) apply.

☐ (a) Applicant petitions for an extension of time under 37 CFR 1.136 (fees: 37 CFR 1.17(a)(1)-(5)) for the total number of months checked below:

<input type="checkbox"/>	one month	\$ 120.00
<input type="checkbox"/>	two months	\$ 460.00
<input type="checkbox"/>	three months	\$1050.00
<input type="checkbox"/>	four months	\$1640.00

☐ The extension fee has already been filled in this application.

☒ (b) Applicant believes that no extension of term is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

Please charge to Deposit Account **08-2623** the sum of \$510.00. At any time during the pendency of this application, please charge any fees required or credit any overpayment to Deposit Account **08-2623** pursuant to 37 CFR 1.25.

☒ I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Date of Deposit: May 1, 2008 OR

☐ I hereby certify that this paper is being submitted electronically via EFS-Web to the Patent and Trademark Office on the date shown below.

Date of submission:

Typed Name: Gregory W. Osterloth

Signature: _____

Respectfully submitted,

Romi Mayder, et al.

By _____

Gregory W. Osterloth
Attorney/Agent for Applicant(s)

Reg. No. 36,232

Date: May 1, 2008

Telephone No. (303) 295-8205



**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES**

Appl. No. : 11/410,699
Appellant : Romi Mayder, et al.
Filed : April 24, 2006
TC/A.U. : 2829
Examiner : Richard Isla Rodas

Confirmation No. : 4586

Docket No. : 10060220-1

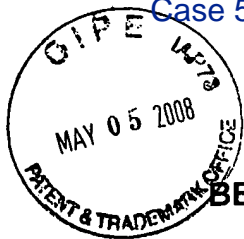
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P.O. Box 1450
Alexandria, VA 22313-1450

APPEAL BRIEF

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**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES**

Appl. No. : 11/410,699 Confirmation No. : 4586
Appellant : Romi Mayder, et al.
Filed : April 24, 2006
TC/A.U. : 2829
Examiner : Richard Isla Rodas

Docket No. : 10060220-1

Mail Stop Appeal Brief – Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPEAL BRIEF

Dear Sir:

This Appeal Brief is submitted in response to the Examiner's Final Office Action dated September 27, 2007.

Appellants filed a Notice of Appeal on January 28, 2008, which was received by the Office on February 1, 2008.

05/05/2008 NNGUYEN1 00000071 082623 11410699
01 FC:1402 510.00 DA

Serial No. 11/410,699
Atty. Dckt. No. 10060220-1

Real Party in Interest

The real party in interest is Verigy (Singapore) Pte. Ltd., a Singapore limited liability company.

Serial No. 11/410,699
Atty. Dckt. No. 10060220-1

Related Appeals and Interferences

There are no related appeals and/or interferences.

Serial No. 11/410,699
Atty. Dckt. No. 10060220-1

Status of Claims

Claims 1-23 are pending, of which claims 1-18 stand withdrawn and claims 19-23 stand rejected. The rejections of claims 19-23 are appealed.

A copy of the claims that are the subject of this appeal is attached as a Claims Appendix to this Appeal Brief.

Serial No. 11/410,699
Atty. Dckt. No. 10060220-1

Status of Amendments

Some minor claim amendments were proposed after issuance of the Final Office Action. All of these amendments have been entered.

Serial No. 11/410,699
Atty. Dckt. No. 10060220-1

Summary of Claimed Subject Matter

Claim 19 recites a method of processing signals between a tester (p. 10, lines 1-12, par. [0026]; FIG. 4, 126) and a plurality of devices under test. The method comprises 1) connecting the tester and the plurality of devices under test with at least one multichip module (p. 7, lines 3-11, pars. [0014]-[0015]; p. 7, line 20 - p. 8, line 9; pars. [0017]-[0019]; p. 9, lines 4-5, par. [0023]; FIG. 1, 102), with each of the at least one multichip module having a plurality of micro-electromechanical switches (p. 7, lines 12-17, par. [0016]; p. 8, lines 10-15, par. [0020]; FIG. 1, 104) between a first set of connectors (106, FIG. 1) to the tester and a se

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Atty. Dckt. No. 10060220-1

Grounds of Rejection to be Reviewed on Appeal

1. Whether claims 19 and 22 should be rejected under 35 USC 103(a) as being unpatentable over Legal (U.S. Pat. No. 5,736,850) in view of Leggett et al. (U.S. Pat. No. 6,098,142).

2. Whether claims 20, 21 and 23 should be rejected under 35 USC 103(a) as being unpatentable over Legal (U.S. Pat. No. 5,736,850) in view of Leggett et al. (U.S. Pat. No. 6,098,142), McCord (U.S. Pat. No. 6,681,869) and Akram (U.S. Pat. No. 6,640,323).

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Atty. Dckt. No. 10060220-1

Argument

1. Claims 19 and 22 should not be rejected under 35 USC 103(a) as being unpatentable over Legal (U.S. Pat. No. 5,736,850) in view of Leggett et al. (U.S. Pat. No. 6,098,142; hereinafter referred to as “Leggett”).

A. Claim 19:

Appellants’ claim 19 recites, in part, the step of “connecting the tester and the plurality of devices under test with at least one multichip module, each of the at least one multichip module having a plurality of micro-electromechanical switches”.

With respect to claim 19, the Examiner asserts that Legal discloses connecting a tester and a plurality of devices under test with “at least one multichip module (216). . . (see lines 59-61 in column 4)”. See, 9/27/2007 Final Office Action, p. 3, sec. 4. However, contrary to the Examiner’s assertion, Legal does not indicate that the “relay matrix 216” is or comprises a multichip module. Column 4, lines 59-61, of Legal state:

Relays 312 may be traditional mechanical type relays. Alternatively, they could be solid state switches or other similar structure.

In the above excerpt, there is no mention by Legal that the relay matrix 216 is (or should be) implemented using a multichip module. Nor does Legal mention that the tester 110 should be connected to devices under test via micro-electromechanical switches on a multichip module. As disclosed by appellants:

In an embodiment, system 124 enables one touchdown testing of 300 mm wafers containing NAND devices to be tested up to 100 MHz by mounting micro-electromechanical multichip modules 102 very close to the DUTs. ***This one touchdown testing cannot be achieved by using mechanical relays or active silicon devices mounted on daughter boards.*** Daughter board mounted on the

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probe cannot achieve the required density of switches because of the space required for connectors.

Appellants' specification, p. 11, par. [0032] (emphasis added).

For the above reasons, appellants assert that Legal fails to teach "connecting [a] tester and [a] plurality of devices under test with at least one multichip module". Given that Leggett also lacks such a teaching, appellants assert that claim 19 should be allowed over the combined teachings of Legal and Leggett.

The Examiner further states, with respect to claim 19, that:

... Legal, teaches that the mechanical switches may also be switches that have control inputs (electrical) or a similar structure (see lines 61-64 in column 4). Legal however, does not explicitly state the use of micro electro-mechanical switches. Nevertheless, it has been held that to be entitled weight in method claims, the recited-structure limitations therein (electro-mechanical switch) must affect the method in a manipulative sense, and not to amount to the mere claiming of a use of a particular structure (in the immediate case, the preferred use of electro-mechanical switches). *Ex parte Pfeiffer*, 1962 C.D. 408 (1961).

9/27/2007 Final Office Action, p. 3, sec. 4.

Although the Examiner relies on *Ex parte Pfeiffer*, appellants note that the Board has consistently refused to apply any *per se rule* in addressing 35 USC 103 rejections - even in the context of method claims. On several occasions, the Board has cited to the non-precedential *In re Ochiai*, which holds:

The use of *per se* rules, while undoubtedly less abhorious than a searching comparison of the claimed invention - including all its limitations - with the teachings of the prior art, flouts section 103 and the fundamental case law applying it. *Per se* rules that eliminate the need for fact-specific analysis of claims and prior art may be administratively convenient for PTO Examiners and the Board. Indeed, they have been sanctioned by the Board as well. But reliance on *per se* rules of obviousness is legally incorrect and must cease. Any such administrative convenience is simply inconsistent with section 103, which, according to *Graham* [*v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966)] and its progeny, entitles an applicant to issuance of an otherwise proper patent unless the PTO established

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Atty. Dckt. No. 10060220-1

that the invention as claimed in the application is obvious over cited prior art, based on the specific comparison of that prior art with claim limitations.

In re Ochiai, 71 F.3d at 1572, 37 USPQ2d at 1133.

In interpreting the phrases “multichip module” and “micro-electromechanical switch”, the Examiner asserts that:

- Finally, applicant does not recite “MEMS”. Applicant recites “micro-electromechanical switches”. Given the broadest reasonable interpretation of the preferred structure the applicant uses to perform the method claim, the limitation recites a mechanical switch that is actuated electrically and which works on the micrometer scale. That is a small mechanical switch that may be operated/switched/actuated electrically.. . .

Likewise, the recitation “multichip module” has been given its broadest reasonable interpretation as a module that is capable of connecting to a plurality of chips.

See, 12/27/2007 Advisory Action.

Although the Examiner is encouraged to interpret appellants' claim limitations broadly, appellants believe it inappropriate to construe the phrase “micro-electromechanical switch” any differently than a MEMS, or to construe a “microchip module” any differently than an MCM. These elements have common and well-understood meanings in the art, and appellants' specification consistently equates the above phrases with their common respective acronyms, without distinguishing the two.

Appellants note that the switches mentioned in their claim 19 are not only “micro-electromechanical switches”, but micro-electromechanical switches provided on a “multichip module”. Not only does Legal fail to disclose the use of micro-electromechanical switches (i.e., MEMS) to connect a tester with devices under test, but Legal also fails to disclose or suggest the use of MEMS that are part of a multichip module (MCM). As mentioned in appellants' specification, MEMS on MCMs may be switched at faster speeds and used at higher temperatures. See, e.g., the discussion in

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 Atty. Dckt. No. 10060220-1

appellants' paragraph [0044] (describing the invention) versus the discussion in appellants' paragraphs [0001] and [0002] (describing past switching methods).

Although the Examiner relies on Leggett's teachings for the proposition that mechanical and electromechanical switches are equivalent, Leggett, like Legal, fails to disclose either MEMS or microchip modules.

With respect to appellants' above discussions of advantages and operating conditions that can be attained using the method set forth in appellants' claim 19, the Examiner's Advisory Action asserts that:

. . . applicant misinterprets the principle that claims are interpreted in light of the specification. Although these virtues (speed or high temperature operability) may be found as examples or embodiments in the specification, they were not claimed explicitly. Nor were the words that are used in the claims defined in the specification, to require these limitations. A reading of the specification provides no evidence to indicate that these limitations must be imported into the claims to give meaning to disputed terms. . .

Appellants disagree with the Examiner's assertion that they are trying to "read into" claim 19 certain limitations and virtues that are not explicitly set forth in claim 19. Rather, appellants merely refer to the specification to illustrate why the differences between what is set forth in claim 19, and the combination of Legal's and Leggett's teachings, are more significant than the Examiner makes them. That is, the method steps, in combination with the structures employed by the method steps, enable appellants' claim 19 to achieve "virtues" that are not achievable by any combination of Legal's and Leggett's methods and apparatus.

In summary, given that neither Legal nor Leggett teach or suggest "connecting [a] tester and [a] plurality of devices under test **with at least one multichip module, each of the at least one multichip module having a plurality of micro-electromechanical switches**", appellants believe claim 19 to be allowable.

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B. Claim 22:

Claim 22 is believed to be allowable because it depends from claim 19, and because Legal and Leggett fail to teach or suggest "mounting each of the at least one multichip module directly on a probe card" (i.e., because neither reference discloses a multichip module or discusses where or how such a module would be used or mounted).

2. Claims 20, 21 and 23 should not be rejected under 35 USC 103(a) as being unpatentable over Legal (U.S. Pat. No. 5,736,850) in view of Leggett et al. (U.S. Pat. No. 6,098,142; hereinafter referred to as "Leggett"), McCord (U.S. Pat. No. 6,681,869) and Akram (U.S. Pat. No. 6,640,323).


Claims 20, 21 and 23 are believed to be allowable, at least, because each of these claims depends from claim 19, and because McCord and Akram fail to disclose that which is missing from the combined teachings of Legal and Leggett. See Section 1 of this Argument for a discussion of what is missing from the combined teachings of Legal and Leggett.

3. Conclusion

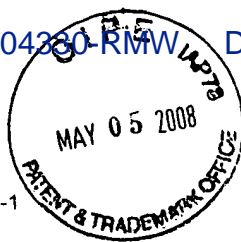
In light of the above arguments, appellants request the allowance of claims 19-23.

Respectfully submitted,
HOLLAND & HART, LLP

By: _____


Gregory W. Osterloth
Reg. No. 36,232
Tel: (303) 295-8205

Serial No. 11/410,699
Atty. Dckt. No. 10060220-1



Claims Appendix

19. A method of processing signals between a tester and a plurality of devices under test, the method comprising:

connecting the tester and the plurality of devices under test with at least one multichip module, each of the at least one multichip module having a plurality of micro-electromechanical switches between a first set of connectors to the tester and a second set of connectors to the plurality of devices under test; and

selectively operating each of the plurality of micro-electromechanical switches to process the signals between individual ones of the first set of connectors to the tester and selected multiple ones of the second set of connectors to the plurality of devices under test.

20. A method in accordance with claim 19, further comprising operating the at least one multichip module at a speed of at least 100 MHz.

21. A method in accordance with claim 19, further comprising operating the multichip module at a temperature of at least 125° C.

22. A method in accordance with claim 19, further comprising mounting each of the at least one multichip module directly on a probe card.

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23. A method in accordance with claim 19, further comprising mounting each of the at least one multichip module directly on a probe card, operating the multichip module at a temperature of at least 125° C, and operating the at least one multichip module at a speed of at least 100 MHz.

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Atty. Dckt. No. 10060220-1

Evidence Appendix

None.

Serial No. 11/410,699
Atty. Dckt. No. 10060220-1

Related Proceedings Appendix

None.

Document code: WFEE

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/410,699	04/24/2006	Romi Mayder	10060220-1	4586
63448	7590	07/25/2008		
Gregory W. Osterloth Holland & Hart, LLP P.O. Box 8749 Denver, CO 80201			EXAMINER ISLA RODAS, RICHARD	
			ART UNIT 2829	PAPER NUMBER
			MAIL DATE 07/25/2008	DELIVERY MODE PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary**Application No.**

11/410,699

Applicant(s)

MAYDER ET AL.

Examiner

RICHARD ISLA RODAS

Art Unit

2829

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 05 May 2008.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-23 is/are pending in the application.
- 4a) Of the above claim(s) 1-18 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 19-23 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 04 April 2006 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

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DETAILED ACTION

Response to Arguments

1. Applicant's arguments in the Notice of Appeal filed 5/5/2008, with respect to the rejection(s) of claim(s) 19-23 under the US Patent to Legal et al. (#5,736,850) in view of the US Patent to Legett et al. (#6,098,142) have been fully considered and are persuasive. Therefore, the rejection of claims 19-23 as stated in the Final Rejection mailed 9/27/2007, has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of the US Patent to Bartlett et al. #5,834,975 and the US Patent to Saia et al. #6,773,962.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. **Claims 19 and 22** are rejected under 35 U.S.C. 103(a) as being unpatentable over the US Patent to Legal (5,736,850) in view of the US Patent to Bartlett et al. #5,834,975 (Bartlett hereinafter) and further in view of the US Patent to Saia et al. #6,773,962 (Saia hereinafter).

In terms of claims 19 and 22, legal teaches in Figure 2A, a method of processing signal between a tester (110) and a plurality of devices under test (cells on top of wafer 122), with at least one multichip module (216) mounted directly on a probe

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card (218), the module having a plurality of mechanical switches (see lines 59-61 in column 4) between a first set of connectors (DRIVER/RECEIVERS) to the tester (110) and a second set of connectors (220) to the plurality of devices under test (cells on wafer 122), and selectively operating each of the plurality of mechanical switches to process (receive and transmit) the signals between individual ones of the first set of connector to the tester and selected multiple ones of the second set of connectors to the plurality of devices under test (The relays provide independent conductive paths between the tester and the probes, said relays can be actuated to connect one of the group of drivers to one of the test sites as explained in lines 50-58, column 4). Legal, teaches that the mechanical switches may also be switches that have control inputs (electrical) or a similar structure (see lines 61-64 in column 4). Legal however, does not explicitly state the use of micro electro-mechanical switches in a multichip module. Nevertheless, it has been held that to be entitled weight in method claims, the recited-structure limitations therein (electro-mechanical switch) must affect the method in a manipulative sense, and not to amount to the mere claiming of a use of a particular structure (in the immediate case, the preferred use of electro-mechanical switches in the multichip module). Ex parte Pfeiffer, 1962 C.D. 408 (1961). Since the method as claimed is not affected by the use of the particular structure, Legal anticipates the method steps.

Nevertheless, the use of micro-electromechanical switches is well known in the art. For example, Bartlett teaches in Figure 1, the use of micro-electromechanical switches (s1, s2, s3... etc) as switching devices for connecting and disconnecting IN

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and PWROUT signals. It would have been obvious to one having ordinary skill in the art at the time the invention was made, to replace the mechanical switches in Legal's device for the micro-electromechanical switches in Bartlett's device, in order to provide switching arrays that are smaller, lighter and consume less power.

Finally, Bartlett doesn't explicitly teach that the micro-electromechanical switches are packaged on multichip modules (MCM). However, multichip module (MCM) packaging of MEMS devices is well known in the art. For example, Saia teaches a method of holding (packaging in) a plurality of MEMS as a multichip module using multichip module techniques (see lines 39-41, col. 1). That is, Saia teaches a method of protecting MEMS by implementing a multichip module that holds a plurality of MEMS. It would have been obvious to one having ordinary skill in the art, to use the teachings of MEMS held by MCM structures, as taught by Saia, to package the micro-electromechanical switches in Bartlett's device inside an MCM structure, in order to protect the fragile micro-electromechanical structures from mechanical and/or chemical attack (as suggested in lines 42-45, col. 1).

4. **Claims 20, 21 and 23** are rejected under 35 U.S.C. 103(a) as being unpatentable over Legal in view of Bartlett in view of Saia and further in view of the US Patent to McCord #6,681,869 and further in view of the US Patent to Akram 6,640,323.

As to claims 20, 21 and 23, Legal in view of Bartlett and McCord substantially teaches all of the claimed steps as discussed above including mounting the multichip module (216) directly on a probe card (218). Legal in view of Bartlett and McCord does

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not explicitly teach however, the step of operating the multichip module at a speed (frequency) of at least 100 MHz. McCord shows that it's well known in the art that to operate a tester (and consequently the module connecting it to the device under test) at and above the rated clock frequency of the device under test (see lines 29-38 in column 10). For instance, when testing a device which working frequency is 533 MHz, is customary to process the signals at frequencies up to 584MHz. It would have been obvious to one of ordinary skill in the art, to operate the multichip module at 100MHz or more when testing devices whose frequency of operation is below such frequency, as taught by McCord, in order to replicate the working conditions of said devices.

Furthermore, McCord is silent as to the preferred temperature of operation of the device. Akram teaches a procedure known as static method of burn-in that consist of applying test signals on devices under test at temperatures of 125 degrees Celsius. Such method comprises the step of applying operating voltages on the devices under test that are much higher than their normal operating voltage, thereby increasing the temperature of the devices under test and removing those devices that fail to withstand the temperature and/or voltage (infant mortality of dies), as explained in lines 21-32 in column 2. It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to apply higher than normal operating voltages on the devices under test of Legal's system (by operating the multichip module to send higher than normal test signals to the devices under test) thereby increasing the temperature of operation to up to 125 degrees, as taught by Akram, in order to detect early failure of

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the devices under test (infant mortality of dies) as suggested by Akram in line 10 of column 2.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Document Number Number-Kind Code e.g. 0500004 A1	Date MM-YYYY	Name	Classification
7,091,765	08-2006	Blak et al.	327/199
2008/0091961	04-2008	Cranford et al.	713/300
7,068,220	06-2006	DeNatale et al.	342/375
6,303,885	10-2001	Hidiwa et al.	200/181

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Richard Isla-Rodas whose telephone number is (571) 272-5056. The examiner can normally be reached on Monday through Friday 8 am to 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ha Nguyen can be reached on (571) 272-1678. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should

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you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Richard Isla-Rodas
July 20, 2008

/Ha T. Nguyen/

Supervisory Patent Examiner, Art Unit 2829

Notice of References Cited	Application/Control No. 11/410,699		Applicant(s)/Patent Under Reexamination MAYDER ET AL.	
	Examiner RICHARD ISLA RODAS		Art Unit 2829	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-7,091,765	08-2006	Bilak et al.	327/199
*	B	US-2008/0091961	04-2008	Cranford et al.	713/300
*	C	US-7,068,220	06-2006	DeNatale et al.	342/375
*	D	US-6,303,885	10-2001	Hichwa et al.	200/181
*	E	US-5,736,850	04-1998	Legal, Dennis Andrew	324/158.1
*	F	US-6,773,962	08-2004	Saia et al.	438/118
*	G	US-6,801,869	10-2004	McCord, Don	702/117
*	H	US-5,834,975	11-1998	Bartlett et al.	330/278
*	I	US-6,640,323	10-2003	Akram, Salman	714/724
	J	US-			
	K	US-			
	L	US-			
	M	US-			


FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Search Notes 	Application/Control No. 11410699	Applicant(s)/Patent Under Reexamination MAYDER ET AL.
	Examiner RICHARD ISLA RODAS	Art Unit 2829

SEARCHED			
Class	Subclass	Date	Examiner
324	754	7/18/2007	RI

SEARCH NOTES		
Search Notes	Date	Examiner
EAST Search (text search only) - updated search, see search history print-out	7/18/2008	RI

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	2	"6681869".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2008/07/20 17:50
L2	7	McCord.in. and tester	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2008/07/20 17:50
L3	2	"6640323".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2008/07/20 17:52
S1	7381	(mem\$1) with chip	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2008/07/11 16:17
S2	9	(mem\$1) with chip same tester	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2008/07/11 16:17
S3	1771	micro with electromechanical with switch\$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2008/07/11 16:19
S4	53	S3 and test same chips	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2008/07/11 16:20
S5	2	"20070247140"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2008/07/11 16:32

S6	14	(mem\$1) with switch\$3 same chip with test\$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2008/07/18 10:07
S7	2	"20070247140"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2008/07/18 10:08
S8	0	(mem\$1) with switch\$3 same MCM same chip with test\$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2008/07/18 10:17
S9	15	(mem\$1) with switch\$3 same MCM and test\$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2008/07/18 10:18
S10	0	probe adj card same MCM same MEMS with switch\$2	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2008/07/18 10:32
S11	2	probe adj card same MCM same MEMS	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2008/07/18 10:32
S12	48	probe adj card same MCM	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2008/07/18 10:32
S13	11	MCM with MEMS with switch\$2	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2008/07/18 11:24
S14	37	MCM same MEMS with switch\$2	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2008/07/18 11:27

S15	3	324/754.ccls. and MEMS with switch\$2	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2008/07/18 11:39
S16	15286	microelectromechanical	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2008/07/18 14:16
S17	360	microelectromechanical adj switch \$2	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2008/07/18 14:16
S18	3	S17 and "324"/\$.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2008/07/18 14:17
S19	3917	\$5electromechanical adj switch\$2	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2008/07/18 14:18
S20	3917	(\$5electromechanical or micro adj electromechanical) adj switch\$2	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2008/07/18 14:20
S21	3	S20 and test same multichip with module	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2008/07/18 14:20
S22	3	(\$5electromechanical or micro adj electromechanical) adj switch\$2 and test and multichip	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2008/07/18 14:21
S23	673	(\$5electromechanical or micro adj electromechanical) adj switch\$2 and test	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2008/07/18 14:21


S24	1	S22 and "324"/\$.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2008/07/18 14:21
S25	104	S19 and "324"/\$.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2008/07/18 14:22
S26	0	microchip adj module same \$7electromechanical adj switch\$2	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2008/07/18 14:30
S27	0	microchip adj module same \$7electromechanical with switch \$2	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2008/07/18 14:31
S28	1	microchip with module same \$7electromechanical with switch \$2	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2008/07/18 14:31
S29	3	multichip with module same \$7electromechanical with switch \$2	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2008/07/18 14:34
S30	47	multichip with module and \$7electromechanical with switch \$2	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2008/07/18 14:34
S31	414	\$7electromechanical with switch \$2 same test\$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2008/07/18 15:28
S32	35	mems with \$7electromechanical with switch\$2 same test\$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2008/07/18 15:31

S33	245	mems with \$7electromechanical with switch\$2 same connect	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2008/07/18 15:40
S34	130	mems with \$7electromechanical with switches with connect	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2008/07/18 15:41
S35	0	mems with \$7electromechanical with switches with connect with chip	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2008/07/18 16:31
S36	14	mems with switches with connect with chip	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2008/07/18 16:31
S37	360	mems with switch\$2 with chip	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2008/07/18 16:49
S38	61	mems with switch\$2 with chip and test	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2008/07/18 16:49
S39	2	"5834975".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2008/07/18 17:27
S40	56	("4598252" "4755769" "5256987" "5578976").PN. OR ("5834975").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2008/07/18 17:31
S41	63	multichip adj module and 324/754.cds.	US-PGPUB; USPAT; USOCR	AND	ON	2008/07/18 17:39
S42	76	multichip adj module and probe adj card	US-PGPUB; USPAT; USOCR	AND	ON	2008/07/18 18:20
S43	7	multichip adj module same probe adj card	US-PGPUB; USPAT; USOCR	AND	ON	2008/07/18 18:20
S44	16	multichip adj module same DUT	US-PGPUB; USPAT; USOCR	AND	ON	2008/07/18 18:26

S45	1	"5834975".pn.	US-PGPUB; USPAT; USOCR	AND	ON	2008/07/18 18:40
S46	71	multichip adj module with mems	US-PGPUB; USPAT; USOCR	AND	ON	2008/07/18 18:42
S47	71	multichip adj module with mems	US-PGPUB; USPAT; USOCR	AND	ON	2008/07/18 18:44
S48	12	("4633573" "5161093" "5353498" "5522006" "5527741" "5731047" "5757072" "5833903" "6150719" "6252229" "6499214").PN. OR ("6773962"). URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2008/07/18 18:58

7/20/2008 6:10:14 PM

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<i>Index of Claims</i> 	Application/Control No. 11410699	Applicant(s)/Patent Under Reexamination MAYDER ET AL.
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✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

<input type="checkbox"/> Claims renumbered in the same order as presented by applicant		<input type="checkbox"/> CPA		<input type="checkbox"/> T.D.		<input type="checkbox"/> R.1.47			
CLAIM		DATE							
Final	Original	07/18/2008							
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	21	✓							
	22	✓							
	23	✓							